SSD2677

Product Information

960 Source x 680 Gate
Active Matrix EPD Display Driver with Controller
for color application

SOLOMON SYSTECH

1 Features

- On chip display RAM
- On-chip booster and regulator for generating VCOM, Gate and Source driving voltage
- 680 outputs gate driver, 960 outputs source driver , 1 output VBD driver for border
- On-chip oscillator
- Embedded OTP to store the waveform settings and parameters
- Support low voltage detect for supply voltage
- Internal Temperature Sensor
- MCU interface: Serial peripheral (3-wire/4-wire)
- Available in COG package

2 ORDERING INFORMATION

Table 2-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SSD2677ZB	Gold Bump Die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 12um
SSD2677ZC	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 12um

3 Pin Description

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to GND, Pull H = connect to V_{DDIO}

Table 3-1: Pin list for SSD2677

Name	Type	Connect to	Description	When not in use
VDD	P	Power Supply	Power Supply pin for the chip	-
VDDIO	P	Power Supply	Power for interface logic pins	-
VCORE	C	Capacitor	Core logic power regulator output pin	
VCORE1	C	Capacitor	Core logic power pin	-
GND	P	GND	Ground	-
GNDA	P	GND	Ground	-
VPP	P	Reserved	Reserved	Open
SCL	I	MPU	Serial clock pin (SPI)	-
SDA	I/O	MPU	Serial data pin (SPI)	-
CSB	I	MPU	Chip Select input pin	-
DC	I	MPU	Data /Command control pin	VDDIO or GND
RST_N	I	MPU	Reset	-
BUSY_N	O	MPU	Busy state output pin	-
BS1	I	VDDIO/GND	Interface Selection Pin	-
M/S#	I	Reserved	Tie to VDDIO.	-
TPE	I/O	Reserved	Connect to TPE	-
TIN	I/O	Reserved	Connect to TIN	-
GDR	I/O	Analog Pin	N-Channel MOSFET Gate Drive Control	-
RESE	I/O	Analog Pin	Current Sense Input for the Control Loop	-
VGH	C	Stabilizing capacitor	Power Supply pin for VSH	-
VGL	C	Stabilizing capacitor	Power Supply pin for VCOM and VSL	-
VSH1	C	Stabilizing capacitor	Positive Source driving voltage	-
VSH2	C	Stabilizing capacitor	Positive Source driving voltage	-
VSL	C	Stabilizing capacitor	Negative Source driving voltage	-
VCOM	C	Panel & Stabilizing capacitor	VCOM driving voltage	-
S [959:0]	O	Panel	Source output pin.	Open
G [679:0]	O	Panel	Gate output pin.	Open
VBD	O	Panel	Border output pin.	Open
TSCL	O	Reserved	Reserved	VSS
TSDA	I/O	Reserved	Reserved	VSS
SYNC0	I/O	Reserved	Reserved	Open
SYNC1	I/O	Reserved	Reserved	Open
CL	NC	NC	Reserved	Open
RSV	NC	NC	Reserved	Open
TP1	NC	NC	Test Pin	Open
TP2	NC	NC	Test Pin	Open
TP3	NC	NC	Test Pin	Open
TP4	NC	NC	Test Pin	Open
TP5	NC	NC	Test Pin	Open
TP6	NC	NC	Test Pin	Open
TP7	NC	NC	Test Pin	Open
TP8	NC	NC	Test Pin	Open
TP9	NC	NC	Test Pin	Open
FB	NC	NC	Test Pin	Open

4 MCU Interface

4.1 MCU Interface selection

The SSD2677 can support 3-wire/4-wire serial peripheral. In the SSD2677, the MCU interface is pin selectable by BS1 shown in Table 4-1.

Note

(1) L is connected to GND

(2) H is connected to V_{DDIO}

Table 4-1 : Interface pins assignment under different MCU interface

MCU Interface	BS1	RST_N	CSB	DC	SCL	SDA
4-wire serial peripheral interface (SPI)	L	Required	CSB	DC	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	CSB	L	SCL	SDA

4.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, DC and CSB. The control pins status in 4-wire SPI in reading/writing command/data is shown in
Table 4-2. The read/write procedure of 4-wire SPI is shown in Figure 4-1.

Table 4-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	L	L
Read/Write data	↑	Data bit	H	L

Note:

(1) L is connected to GND and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of DC should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to DC pin.

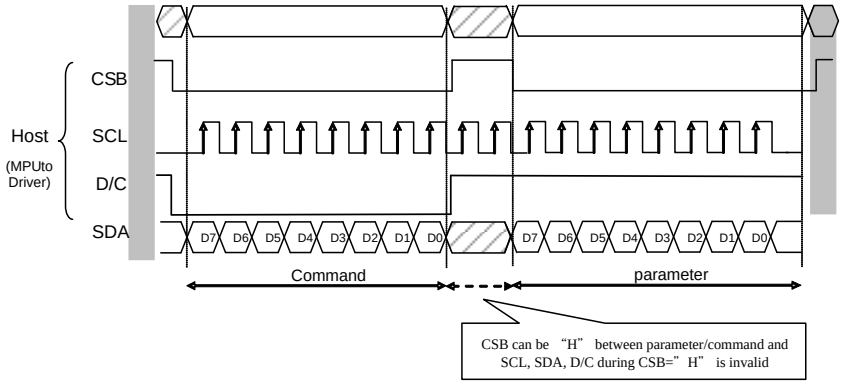


Figure 4-1 : Read/Write procedure in 4-wire SPI mode

4.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CSB. The operation is similar to 4-wire SPI while DC pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 4-3. The read/write procedure of 3-wire SPI is shown in Figure 4-2.

In the read/write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is DC bit, D7 bit, D6 bit to D0 bit. The first bit is DC bit which determines the following byte is command or data. When DC bit is 0, the following byte is command. When DC bit is 1, the following byte is data. Table 4-3 shows the write procedure in 3-wire SPI

Table 4-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	Tie LOW	L
Read/Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to GND and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

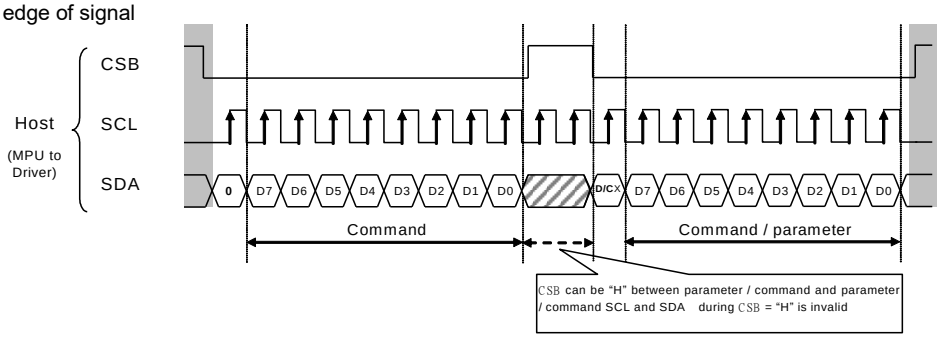


Figure 4-2 : Read/Write procedure in 3-wire SPI mode

5 Command Table Description

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>00</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PSR</td><td>Panel Setting Register
A[7:0] = 0Fh [POR]
B[7:0] = 09h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[7:6] ~ RES[1:0]
Display Resolution setting (source x gate)
00b: 960 x 680 (Default)
01b: 960 x 672
10b: 960 x 640
11b: 880 x 528

A[3] ~ UD
Gate Scan Direction:
0: Scan down.
First line to Last line: Gn-1 … G0
1: Scan up. (Default)
First line to Last line: G0 … Gn-1

A[2] ~ SHL
Source Shift Direction:
0: Shift left.
First data to Last data: Sn-1 … S0
1: Shift right. (Default)
First data to Last data: S0 … Sn-1

A[1] ~ SHD_N
Booster and Regulator Switch:
0: PON / POF command will not execute
1: PON / POF command will execute (Default)

A[0] ~ RST_N
Soft Reset:
0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled.
1: Normal operation (Default).
BUSY_N signal will become “0” until Soft reset is finished.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td><td></td><td></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>PWR</td><td>Power setting Register
A[5:0] = 07h [POR]
B[7:0] = F0h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[2:0] = 111 [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>B_1</td><td>B_0</td><td></td><td>B[1:0] ~ VGPN [1:0]
Internal VGH / VGL Voltage Level Selection:
<table>
<tr><th>VGPN [1:0]</th><th>Gate Voltage Level</th></tr>
<tr><td>00</td><td>VGH=20V,VGL=-20V (Default)
VSH=15V, VSL=-15V</td></tr>
<tr><td>01</td><td>VGH=17V ,VGL=-17V
VSH=15V, VSL=-15V</td></tr>
<tr><td>10</td><td>VGH=15V,VGL=-15V
VSH=15V, VSL=-15V</td></tr>
<tr><td>11</td><td>Reserved.</td></tr>
</table></td></tr>
</table>

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	02	0	0	0	0	0	0	1	0	POF	Power OFF Command Register
0	1		0	0	0	0	0	0	0	0		After power off command, driver will power off based on the Power OFF Sequence, then BUSY_N signal will become “0”. The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off. SD output will base on previous condition. *Remark: POF works at PON only
0	0	04	0	0	0	0	0	1	0	0	PON	Power ON Command Register After the Power ON command, driver will power on based on the Power ON Sequence. After power on command and all power sequence are ready, then BUSY_N signal will become “1”. * Remark: PON Include booster on, VSHx/VSLx regulator on With default BTST, timing is >80ms
0	0	06	0	0	0	0	0	1	1	0	BTST	VGH Booster Soft Start Setting Register (for VGH) A[6:0] = 0Fh [POR] B[6:0] = 8Bh [POR] C[6:0] = 93h [POR] D[6:0] = A1h [POR] A[3:2] ~ T_VGHSSA [1:0] = 11 (Default) VGH booster soft start Phase A duration A[1:0] ~ T_VGHSSB [1:0] = 11 (Default) VGH booster soft start Phase B duration B[6:4] ~ VGHSSA_DRV [2:0], = 000 (Default) VGH Phase A Driving Strength C[6:4] ~ VGHSSB_DRV [2:0], = 001 (Default) VGH Phase B Driving Strength D[6:4] ~ VGHSSC_DRV [2:0] = 001 (Default) VGH Phase C Driving Strength 000~011 for Driving Strength 0~3. Others are reserved. B[3:0] ~ VGHSSA_OFFT[[3:0], = 1011 (Default) VGH Phase A Minimum OFF Time C[3:0] ~ VGHSSB_OFFT[[3:0], = 0011 (Default) VGH Phase B Minimum OFF Time D[3:0] ~ VGHSSC_OFFT[[3:0], = 0011 (Default) VGH Phase C Minimum OFF Time 0000~1111 for Minimum OFF Time (setting) OFFH0 to OFFHF.
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		1	D_6	D_5	D_4	D_3	D_2	D_1	D_0		

	Soft Start Phase Period (ms)
00	10
01	20
10	30
11	40

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>07</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>DSLP</td><td rowspan="2">Deep Sleep Register
This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion.
The only one parameter is a check code, the command would be executed if check code is A5h.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>17</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>AUTO</td><td>Auto Sequence Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>This command makes the chip enter the auto sequence Single-chip application ONLY.
Auto Sequence Option
0xA5: Start Auto Sequence (PON > DRF > POF)
0xA7: Start Auto Sequence (PON > DRF > POF > DSLP).
Others: No effect
BUSY_N signal will become “0” until Auto Sequence is finished.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DTM</td><td rowspan="5">Data Start transmission Register
This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.

KPixel[1:0] Source Driver Output
<table><tr><td></td><td>DDX=1 (Default)</td></tr><tr><td>00b</td><td>Gray 0</td></tr><tr><td>01b</td><td>Gray 1</td></tr><tr><td>10b</td><td>Gray 2</td></tr><tr><td>11b</td><td>Gray 3</td></tr></table>After issue this command, the host must send at least 1 byte data to the device.</td></tr>
<tr><td colspan="10">2 bit per pixel</td></tr>
<tr><td>0</td><td>1</td><td></td><td colspan="2">KPixel1 [1:0]</td><td colspan="2">KPixel2 [1:0]</td><td colspan="2">KPixel3 [1:0]</td><td colspan="2">KPixel4 [1:0]</td></tr>
<tr><td>:</td><td></td><td></td><td colspan="2"></td><td colspan="2"></td><td colspan="2"></td><td colspan="2"></td></tr>
<tr><td>0</td><td>1</td><td></td><td colspan="2">KPixel (4M-3) [1:0]</td><td colspan="2">KPixel (4M-2) [1:0]</td><td colspan="2">KPixel (4M-1) [1:0]</td><td colspan="2">KPixel (4M) [1:0]</td></tr>
<tr><td colspan="10"></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>DRF</td><td rowspan="2">Display Refresh Command Register
After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. LUT can define DCVCOM/ACVCOM.
After Display Refresh command, BUSY_N signal will become “0” until display update is finished.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>40</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>TSC</td><td rowspan="2">Temperature Sensor Command Register
This command enables internal temperature sensor. BUSY_N will go low during temperature sensor is under operation. Then the temperature value can be read in 1degC step
A[7:0] ~ TS [7:0]
<table><tr><td>TS [7:0]</td><td>Return Value(degC)</td></tr><tr><td>E7h</td><td>-25</td></tr><tr><td>…</td><td>…</td></tr><tr><td>FFh</td><td>-1</td></tr><tr><td>00h</td><td>0</td></tr><tr><td>01h</td><td>1</td></tr><tr><td>…</td><td>…</td></tr><tr><td>19h</td><td>25</td></tr><tr><td>…</td><td>…</td></tr><tr><td>31h</td><td>49</td></tr><tr><td>32h</td><td>50</td></tr></table></td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>50</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>CDI</td><td>A[7:0] = 97h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>A[7:5]~VBD [2:0]
Border Output Selection:<table><tr><td></td><td>DDX=1</td></tr><tr><td>VBD[2:0]</td><td>LUT (Default)</td></tr><tr><td>000</td><td>Gray 0</td></tr><tr><td>001</td><td>Gray 1</td></tr><tr><td>010</td><td>Gray 2</td></tr><tr><td>011</td><td>Gray 3</td></tr><tr><td>100</td><td>HIZ(Default)</td></tr></table></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>61</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>TRES</td><td>Resolution setting Register
This command defines alternative resolution</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_9</td><td>A_8</td><td></td><td rowspan="4">A[7:0] ~ HRES[9:0]
Horizontal Display Resolution
Remark: Horizontal resolution should be 4-multiple.
B[8:0] ~ VRES[9:0]
Vertical Display Resolution

e.g. HRES= 3C0h, VRES= 2A8h<table><tr><td>UD,SHL</td><td>Source and gate sequence</td></tr><tr><td>00</td><td>S679,G959 to S0,G0</td></tr><tr><td>01</td><td>S0, G959 to S679,G0</td></tr><tr><td>10</td><td>S679,G0 to S0, G959</td></tr><tr><td>11</td><td>S0,G0 to S679, G295</td></tr></table>Remark:
1) Both PSR.RES & TRES command can set panel resolution. Priority will be given to the last received PSR or TRES command.
2) VRES[8:0] >= 120</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_9</td><td>B_8</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td><td></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>70</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>REV</td><td>Chip Revision Register
The command is to read the ID
A[7:0] = 07h [POR]</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>80</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>AMV</td><td>Auto Measurement VCOM Register
This command implements related VCOM sensing setting.
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>0</td><td>A_0</td><td></td><td>A[7:6] ~ P[1:0]
Number of sensing Points
00: 2 (Default)
01: 4
10: 8
11: 16

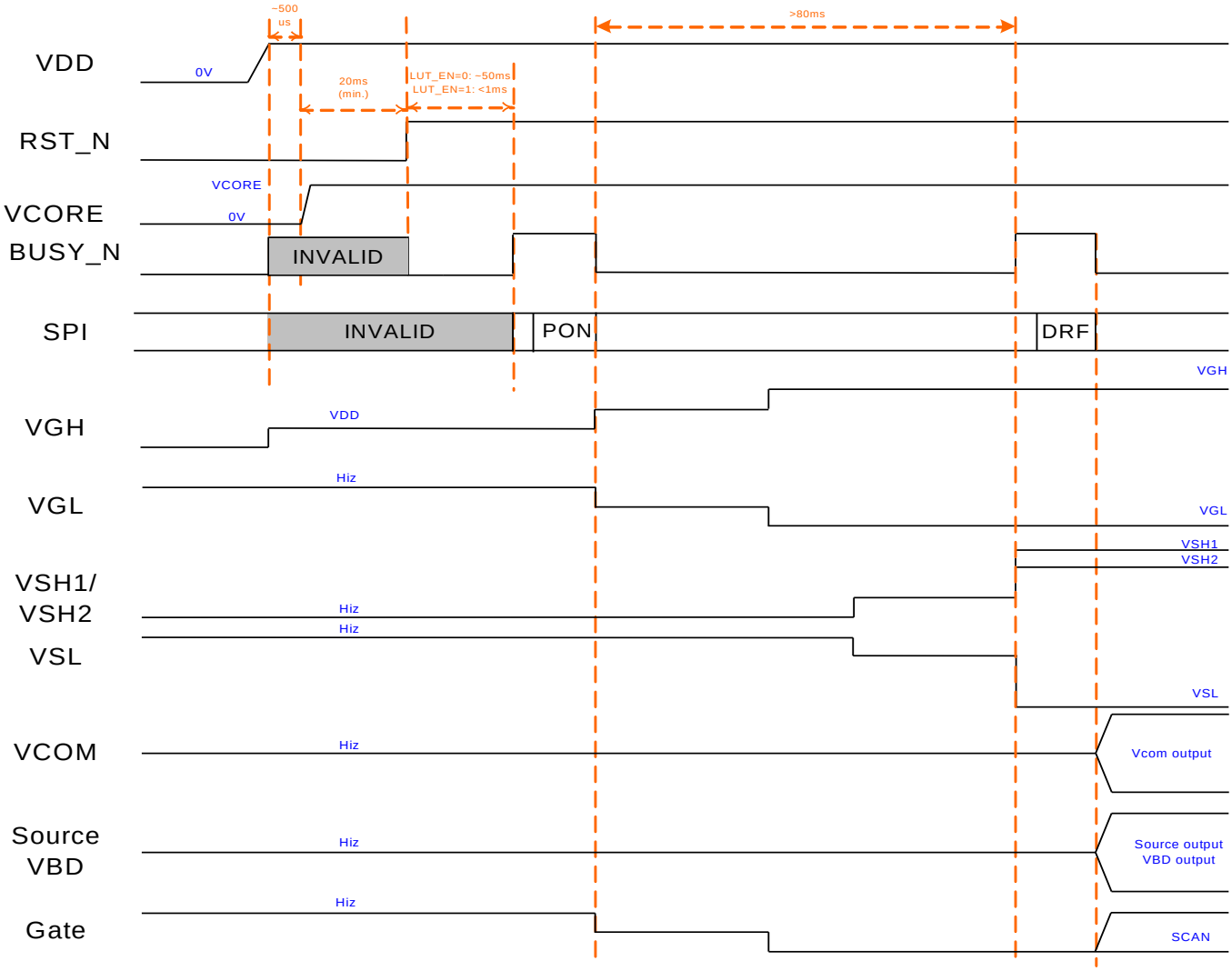
A[5:4] ~AMVT[1:0]
Auto Measure Vcom Time:
Sensing Time
00: 5 sec. (Default)
01: 10 sec.
10: 15 sec.
11: 20 sec.

A[0] ~ AMVE
Auto Measure Vcom Enable (/Disable):
0: Disabled (Default)
1: Enabled
Requirement:
1) AMV works at PON only
2) BUSY_N signal will become “0” until Vcom sensing is finished.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>81</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>VV</td><td>Auto Measurement VCOM Register
This command gets the Vcom value after AMV.</td></tr>
<tr><td>1</td><td>1</td><td></td><td>1</td><td>0</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[5:0] ~ VV[5:0]:
Vcom read Value , valid range from -0.2V to -4.0V.<table><tr><td>VV[5:0]</td><td>Vcom read value</td></tr><tr><td>00h</td><td>Reserved</td></tr><tr><td>04h</td><td>-0.2V</td></tr><tr><td>08h</td><td>-0.4V</td></tr><tr><td>0Ch</td><td>-0.6V</td></tr><tr><td>10h</td><td>-0.8V</td></tr><tr><td>…</td><td>…</td></tr><tr><td>50h</td><td>-4.0V</td></tr><tr><td>others</td><td>Reserved</td></tr></table></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>82</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>VDCS</td><td>VCM_DC Setting Register
This command sets VCOM_DC value.
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>0</td><td>0</td><td></td><td>A[7] ~ OTP_VCM
Vcom follow VDCS after RESET.
0: Disable (Default), auto load from OTP if it is valid.
1: Enable, VCOM value from the VDCS[6:0]
A[6:0] ~ VDCS[6:0]:
VCOM_DC Setting, 0.2V step from -0.2V to -4.0V.<table><tr><td>VDCS [6:0]</td><td>VCOM_DC Setting</td></tr><tr><td>00h</td><td>Reserved</td></tr><tr><td>04h</td><td>-0.2V</td></tr><tr><td>08h</td><td>-0.4V</td></tr><tr><td>0Ch</td><td>-0.6V</td></tr><tr><td>10h</td><td>-0.8V</td></tr><tr><td>…</td><td>…</td></tr><tr><td>50h</td><td>-4.0V</td></tr><tr><td>others</td><td>Reserved</td></tr></table></td></tr>
</table>

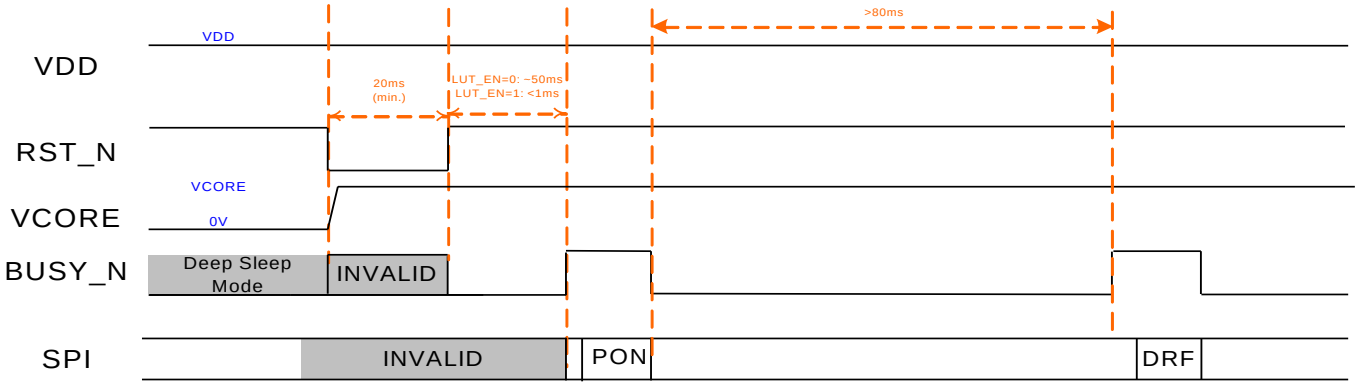
R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	90	1	0	0	1	0	0	0	0	PGM	Program Mode This command is to set OTP program mode After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leave the program mode BUSY_N signal will become 0 until PGM mode is ready.
0	0	91	1	0	0	1	0	0	0	1	APG	Active Program This command is to execute OTP program After this command is issued, the chip would program the OTP. BUSY_N signal will become 0 until the programming is completed. Requirement: In PON mode with internal programming power.
0	0	92	1	0	0	1	0	0	1	0	ROTP	Read OTP Data This command is to read the OTP content from SRAM. The 1st byte read is dummy byte. The 2nd byte read is the content of Address 0 in OTP The N+1th byte read is the content of Address n in OTP After issue this command, the host must read at least 1 byte data from the device.
1	1		1st ~ dummy 2nd ~ N+1th Parameter									
0	0	E3	1	1	1	0	0	0	1	1	PWS	Power Saving Register This command is sets for saving power VCOM/Source power saving during display refresh period. A[7:0] = 65h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

6 Display on/off Sequence

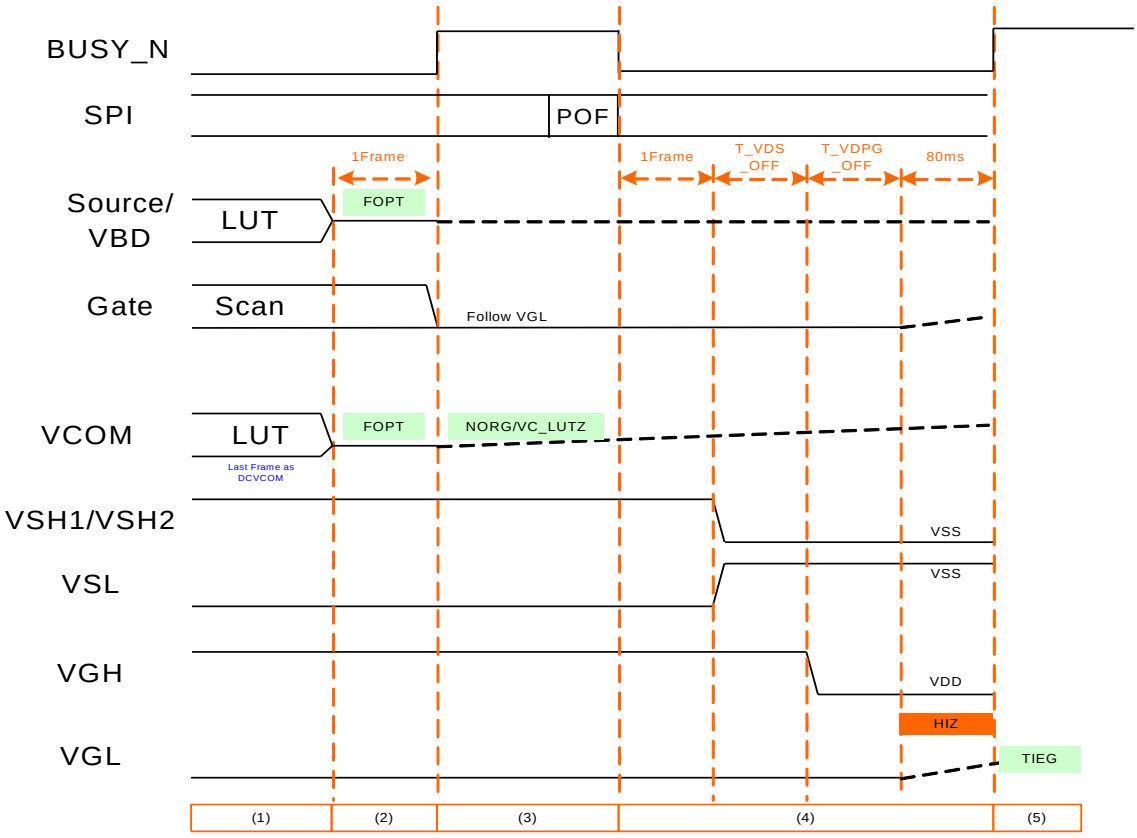
6.1 Display on sequence from VDD power on



6.2 Display on sequence from deep sleep mode



6.3 Display off Sequence Display



7 Absolute Maximum Rating

Table 7-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-30 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VDD be constrained to the range GND < VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either GND or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

8 Electrical Characteristics

The following specifications apply for: GND=0V, VDD=3.0V, T_{OPR}=25ºC.

Table 8-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	VDD supply operation voltage	VDD		2.3	3.0	3.6	V
V_{COM_DC}	VCOM_DC output voltage	VCOM		-4.0	-	-0.2	V
dV_{COM_DC}	VCOM_DC output voltage deviation	VCOM	No output load	-200	-	200	mV
V_{COM_AC}	VCOM_AC output voltage	VCOM		V_{SL}	V_{COM_DC}	V_{SH}	V
V_{GATE}	Gate output voltage	G0~G679		-20	-	+20	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage	G0~G679		-	-	40	V
VSH	Positive Source output voltage	VSH1		+3		+15	V
VSH2	Positive Source output voltage	VSH2		+3		+15	V
dV_{SH}	VSH1/VSH2 output voltage deviation	VSH1/ VSH2	No output load	-200	-	200	mV
V_{SL}	Negative Source output voltage	VSL		-15		-3	V
dV_{SL}	VSL output voltage deviation	VSL	No output load	-200	-	200	mV
V_{IH}	High level input voltage	SDA SCL, CSB, DC, RST_N, BS1		0.8V_{DDIO}	-	-	V
V_{IL}	Low level input voltage			-	-	0.2V_{DDIO}	V
V_{OH}	High level output voltage	SDA, BUSY_N,	IOH = -100uA	0.8V_{DDIO}	-	-	V
V_{OL}	Low level output voltage		IOL = 100uA	-	-	0.2V_{DDIO}	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{PP}	OTP Program voltage	VPP		8.1	8.3	8.5	V
Islp_VDD	Sleep mode current	VDD	- DC/DC off - No clock - No output load - MCU interface access - RAM data access	-	TBD	TBD	uA
Idslp_VDD	deep sleep current	VDD	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data	-	TBD	TBD	uA
Iopr_VDD	Operating Mode current	VDD	VDD=3V After PON Command VGH=20V VGL=-VGH VSH=15V VSH2=15V VSL=-15V VCOM = -2V No waveform transitions. No output load No RAM read/write	-	TBD	-	mA
V_{GH}	Operating Mode Output Voltage	VGH		19.5	20	20.5	V
V_{SH}		VSH1		14.8	15	15.2	V
V_{SH2}		VSH2		14.8	15	15.2	V
V_{SL}		VSL		-15.2	-15	-14.8	V
V_{COM}		VCOM		-2.2	-2	-1.8	V

9 AC Characteristics

9.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - GND = 2.3V to 3.6V, T_{OPR} = 25°C, CL=20pF

Table 9-1 : Serial Peripheral Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB select setup time	TBD			ns
t_{SCH}	CSB select hold time	TBD			ns
t_{SCC}	CSB deselect setup time	TBD			ns
t_{CHW}	CSB deselect hold time	TBD			ns
t_{SCYCW}	Serial clock cycle (Write)	TBD			ns
t_{SHW}	SCL “H” pulse width (Write)	TBD			ns
t_{SLW}	SCL “L” pulse width (Write)	TBD			ns
t_{SCYCL}	Serial clock cycle (Read)	TBD			ns
t_{SHR}	SCL “H” pulse width (Read)	TBD			ns
t_{SLR}	SCL “L” pulse width (Read)	TBD			ns
t_{SDS}	Data setup time	TBD			ns
t_{SDH}	Data hold time	TBD			ns
t_{ACC}	Access time			TBD	ns
t_{OH}	Output disable time	TBD			ns

Note: All timings are based on 20% to 80% of VDDIO-GND

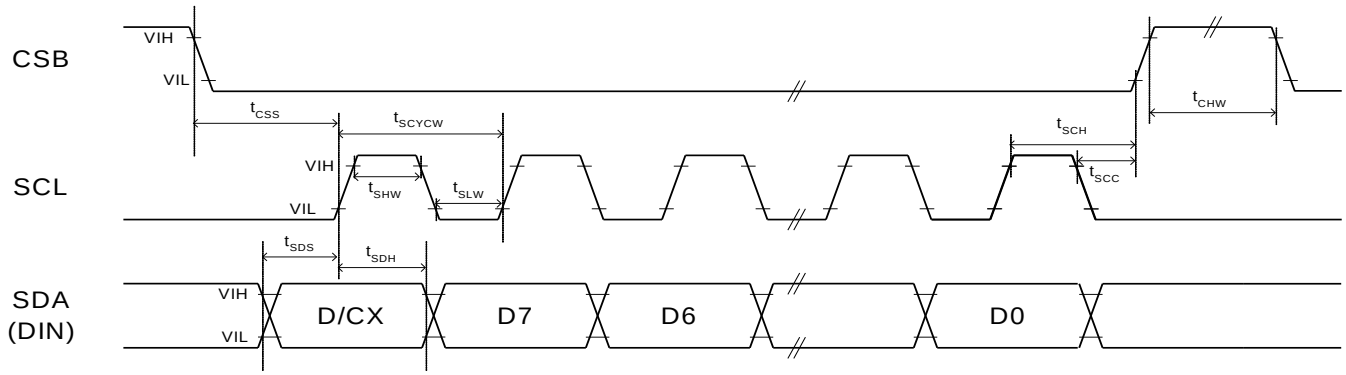


Figure 9-1: 3-wire serial interface characteristics (write mode)

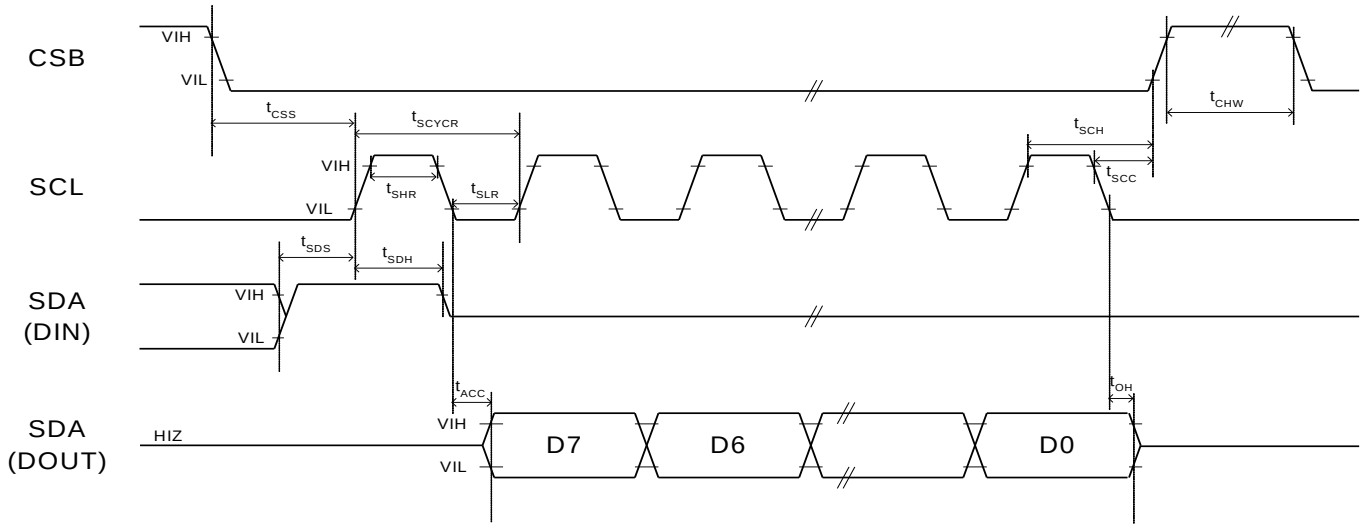


Figure 9-2: 3-wire serial interface characteristics (read mode)

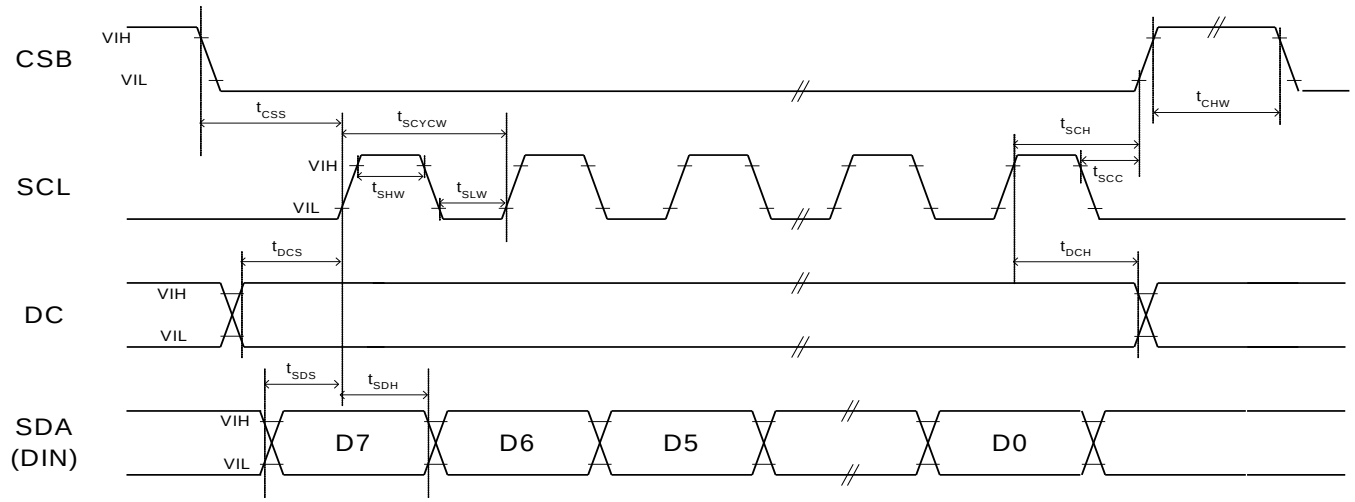


Figure 9-3: 4-wire pin serial interface characteristics (write mode)

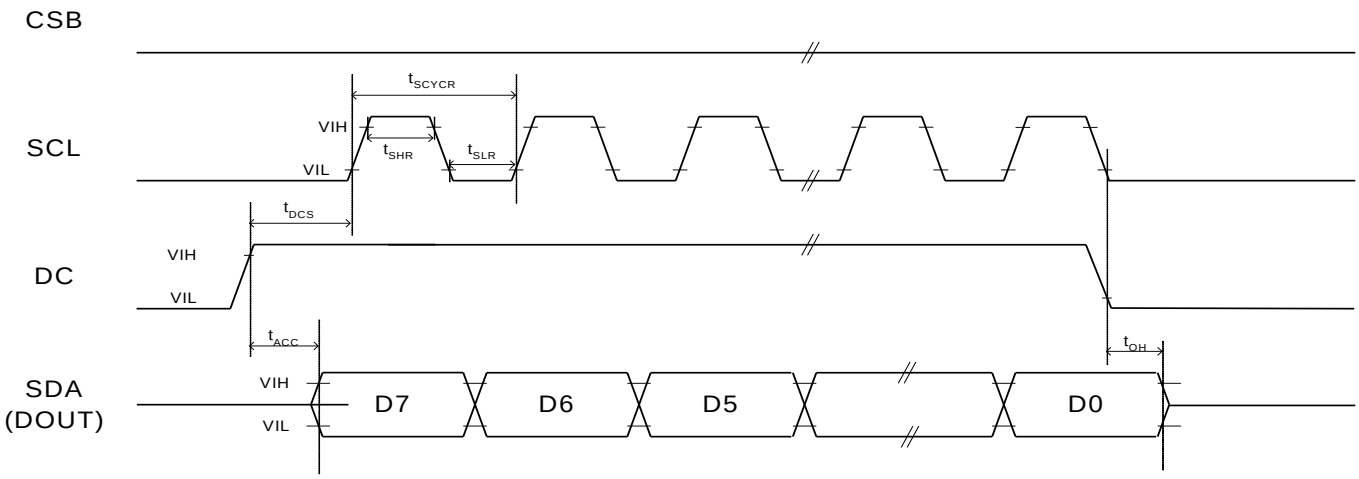


Figure 9-4: 4-wire serial interface characteristics (read mode)

10 Application Circuit

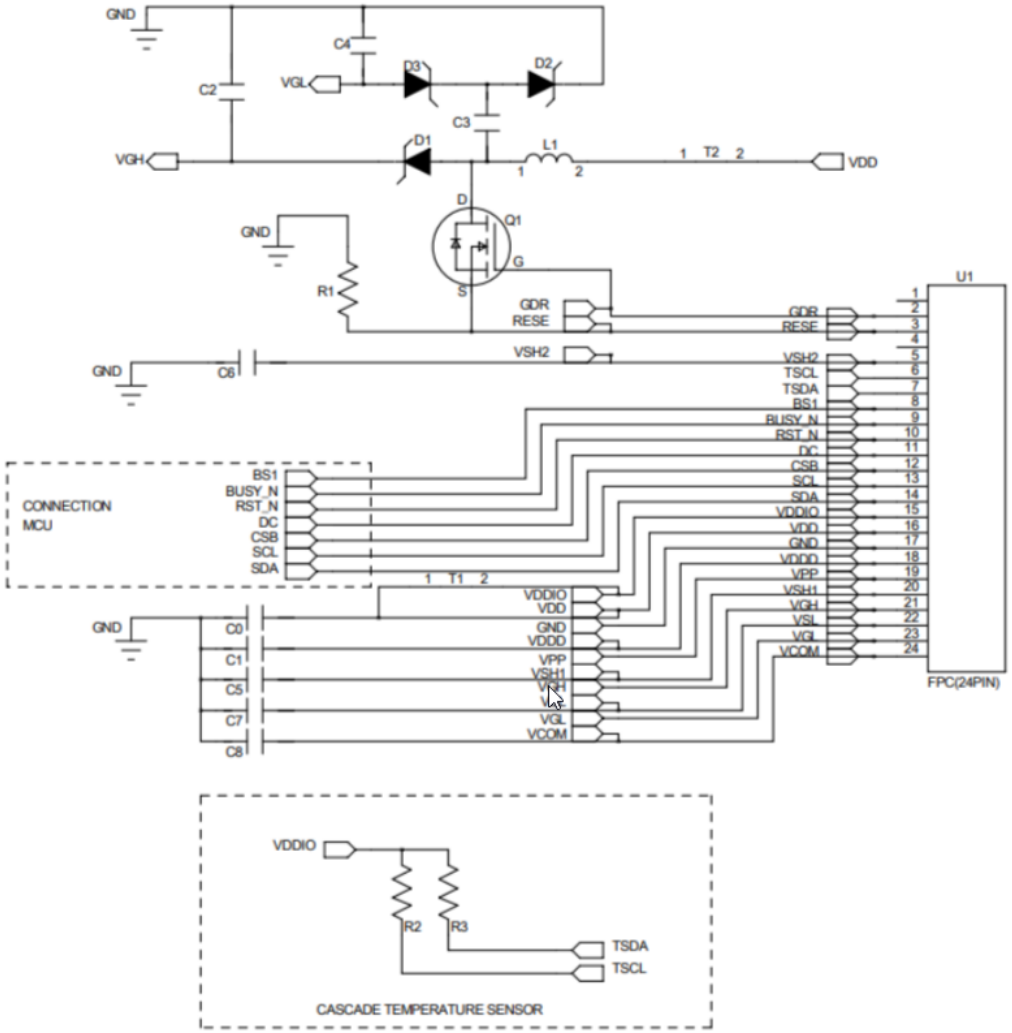


Figure 10-1: SSD2677 application circuit

Table 10-1: Component list for SSD2677 application circuit

Part Name	Value	Requirements/Reference Part
C0	4.7uF	X5R/X7R; Voltage Rating : 6V or 25V
C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	4.7uF	0805; X5R/X7R; Voltage Rating: 25V
C8	1uF	0805; X7R; Voltage Rating: 25V
R1	2.2 ohm	0805; 1%
R2, R3	Open	Connect to VSS in single chip application
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥ 500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≤ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

Remarks:

1) The recommended component value and reference part in Table 10-1 is subject to change depending on panel loading.
2) Customer is required to review if the selected component value and part is suitable for their application.

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