JADARD

JD79665AA

Data Sheet

All-in-one driver with
TCON for Color application

Version 1.0.0
2023/08/25

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All-in-one driver with TCON for Color application

1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 2-bit output per pixel. The timing controller provides control signals for the source driver and gate drivers.

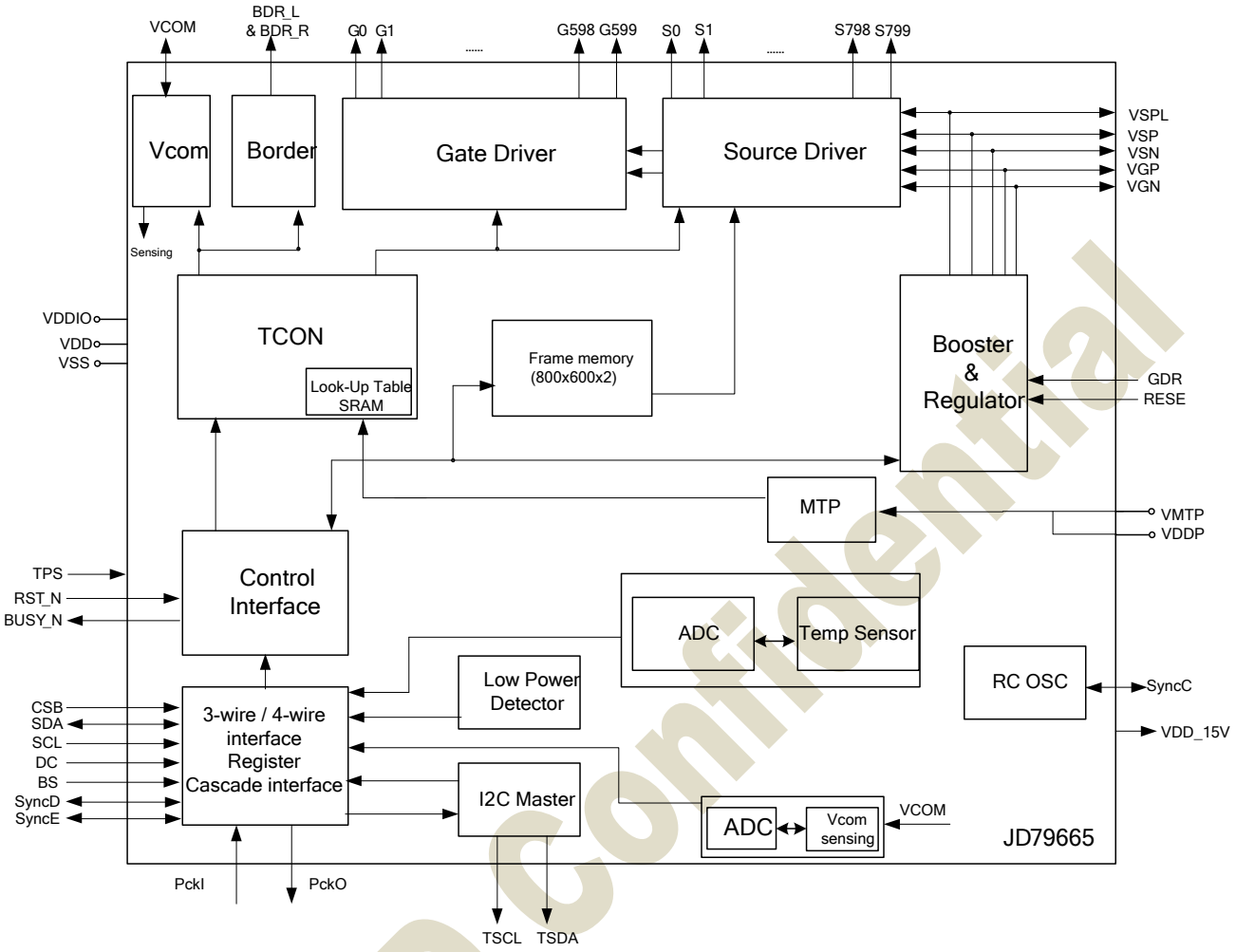
The DC-DC controller allows to generate the source output voltage VSP_0/VSN_0(+/-15V),VSP_1/VSPL_0/VSPL_1/VSN_1 (+/-3V~+/-15V) and VGP/VGN(+/-20V, +/-17V, +/-15V, +/-10V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire(SPI) serial.

2. FEATURES

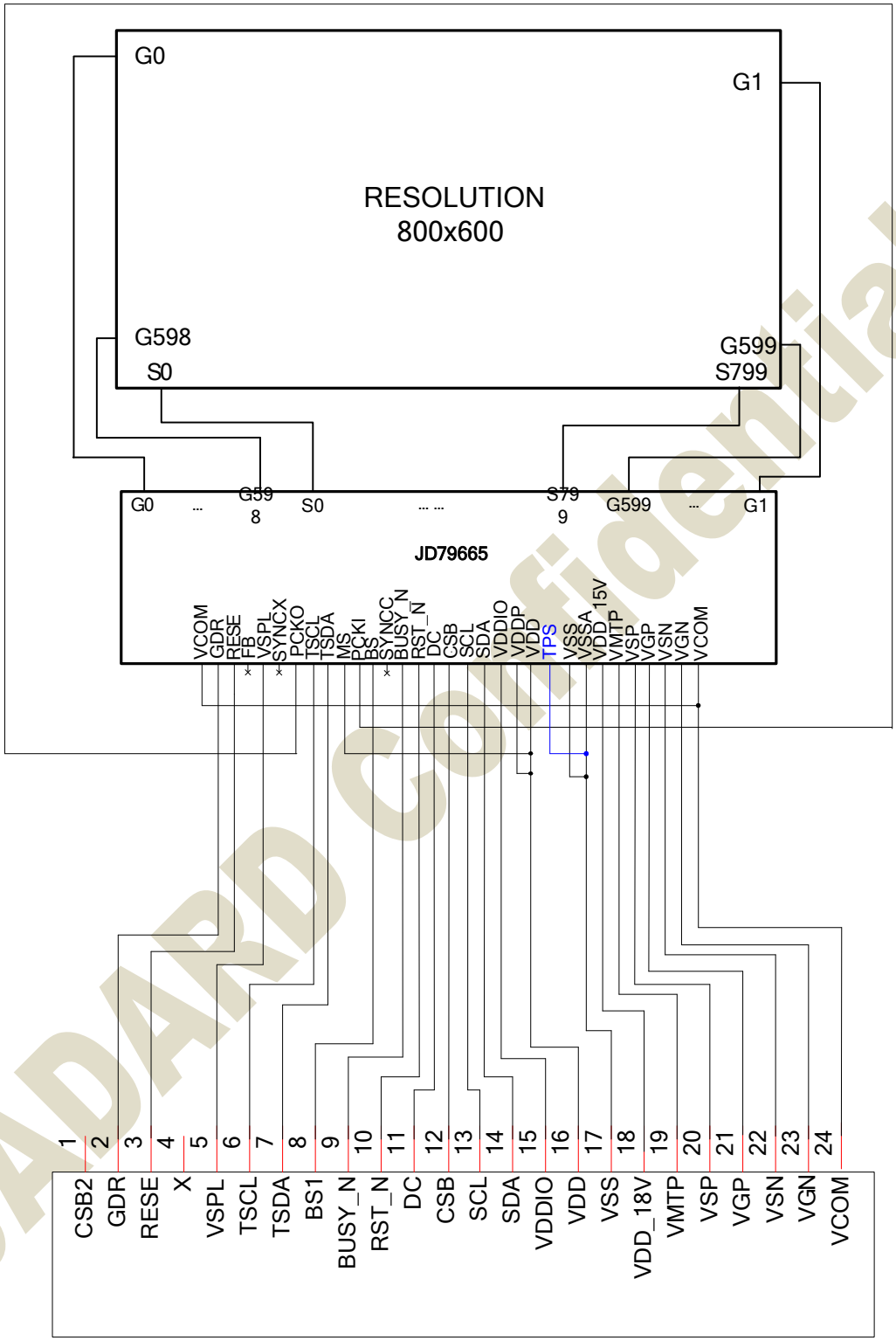
- System-on-chip (SOC) for color application
- Timing controller support several all resolution (maximum resolution 800x600)
- Support source & gate driver function:
  - 800 Outputs source driver with 2-bit black/white/red/yellow per pixel:
    - Output dynamic range(Voltage step:100mV):
      - Mode 0: 0V & VSP_0(+15V) & VSN_0(-15V) & VSPL_0(+3V~+15V)
      - Mode 1: 0V & VSP_1 (+3V ~ +15V) & VSN_1(-3V ~ -15V) & VSPL_1 (+3V ~ +15V)
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame)
    - Left and Right shift capability
  - 600 Output gate driver:
    - Output dynamic range: VGP and VGN(+/-20V, +/-17V, +/-15V, +/-10V)
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (7-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: 800 x 600 x 2 bit SRAM
- Built in temperature sensor:
  - On-Chip: -25 ^{o}C ~50 ^{o}C ± 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}< 2.2V~2.5V)
- PLL : On-chip RC oscillator
- 3-wire/4-wire (SPI) serial interface for system configuration
- Digital supply voltage: 2.3~3.6V
- 4.0 K-byte MTP for LUT, User command
- Partial update

- Support cascade
- Support N-Type and P-Type TFT Panel
- Package-COG

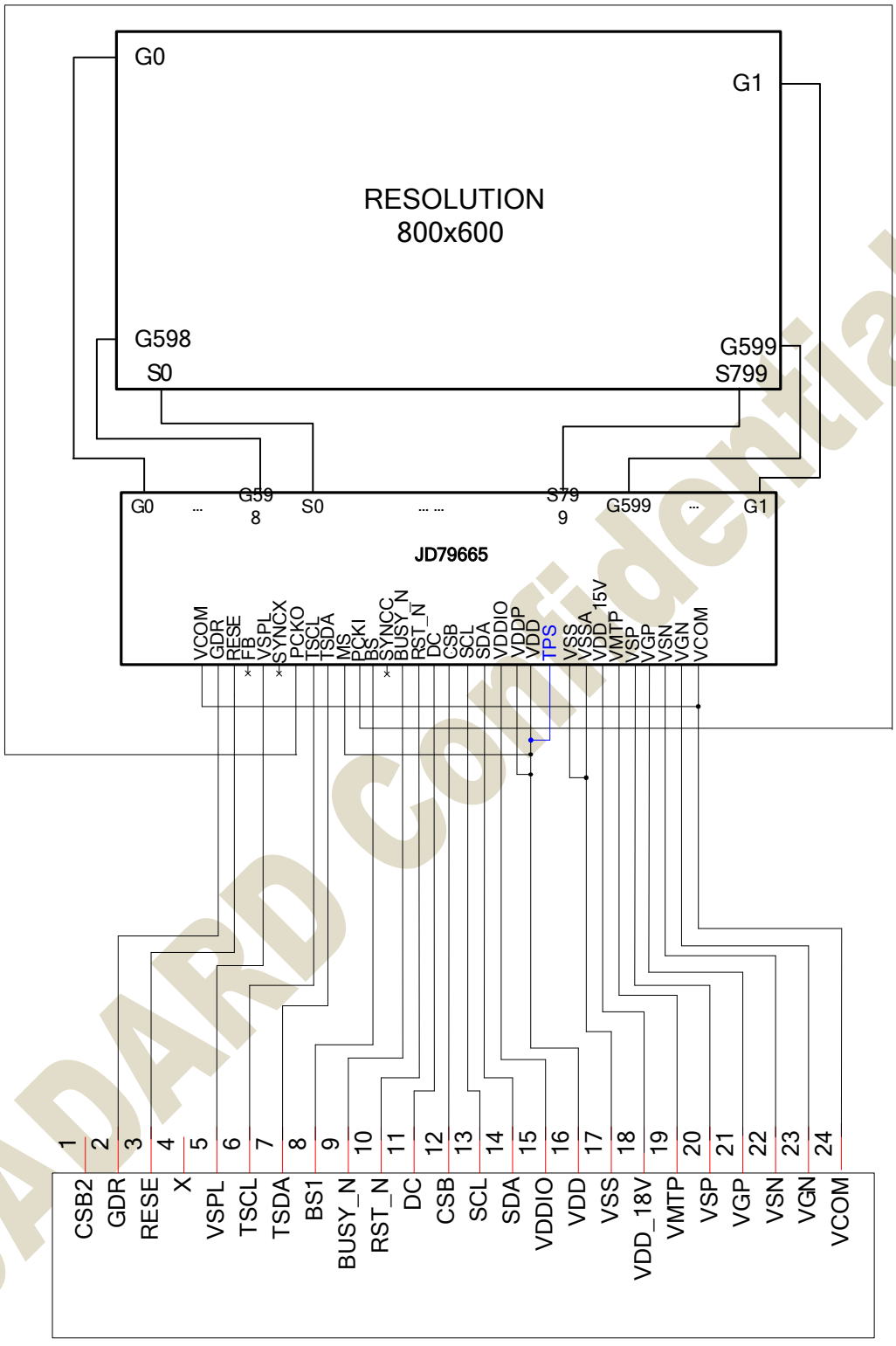
3. BLOCK DIAGRAM



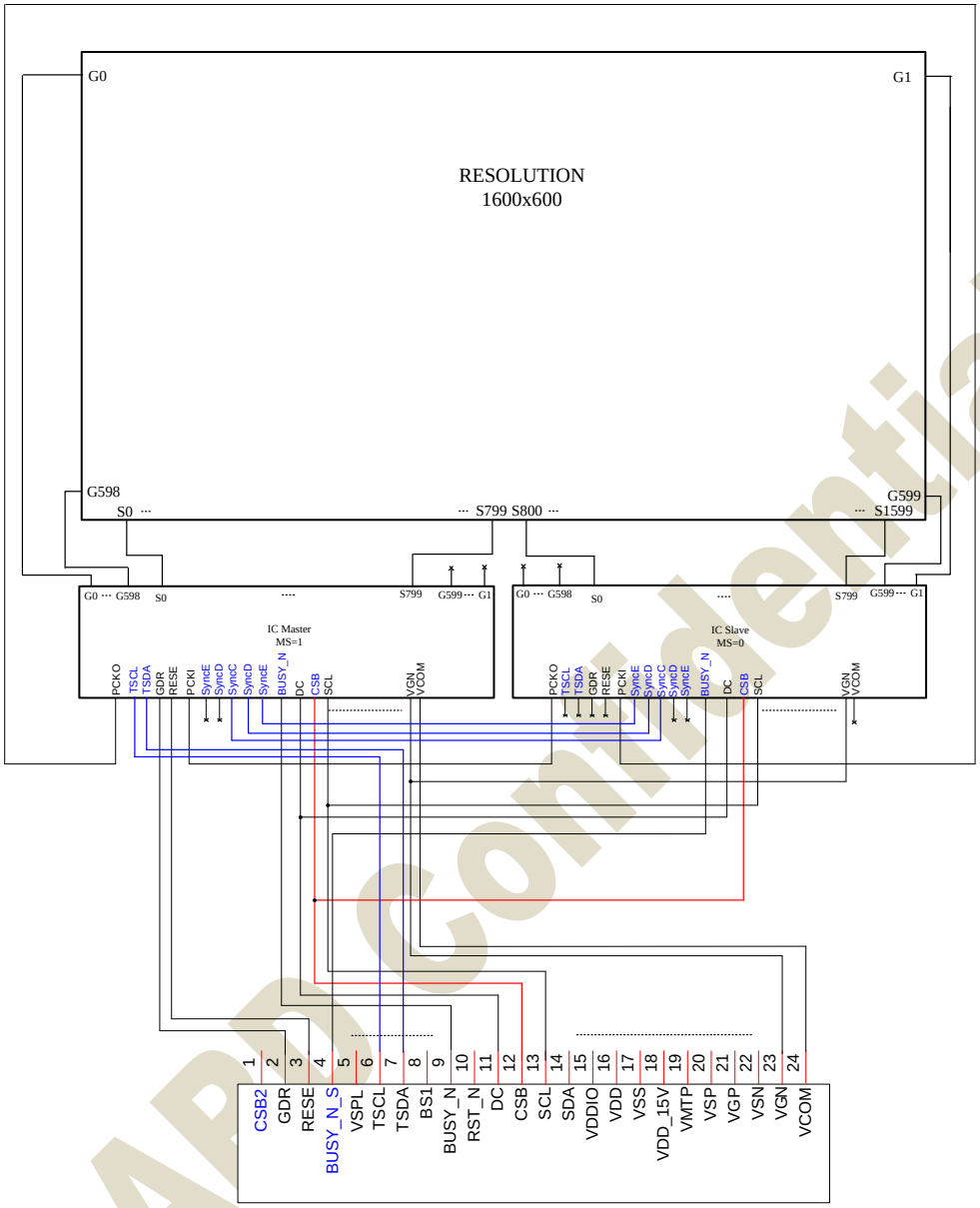
Normal type (TPS=Low, N-Type TFT)



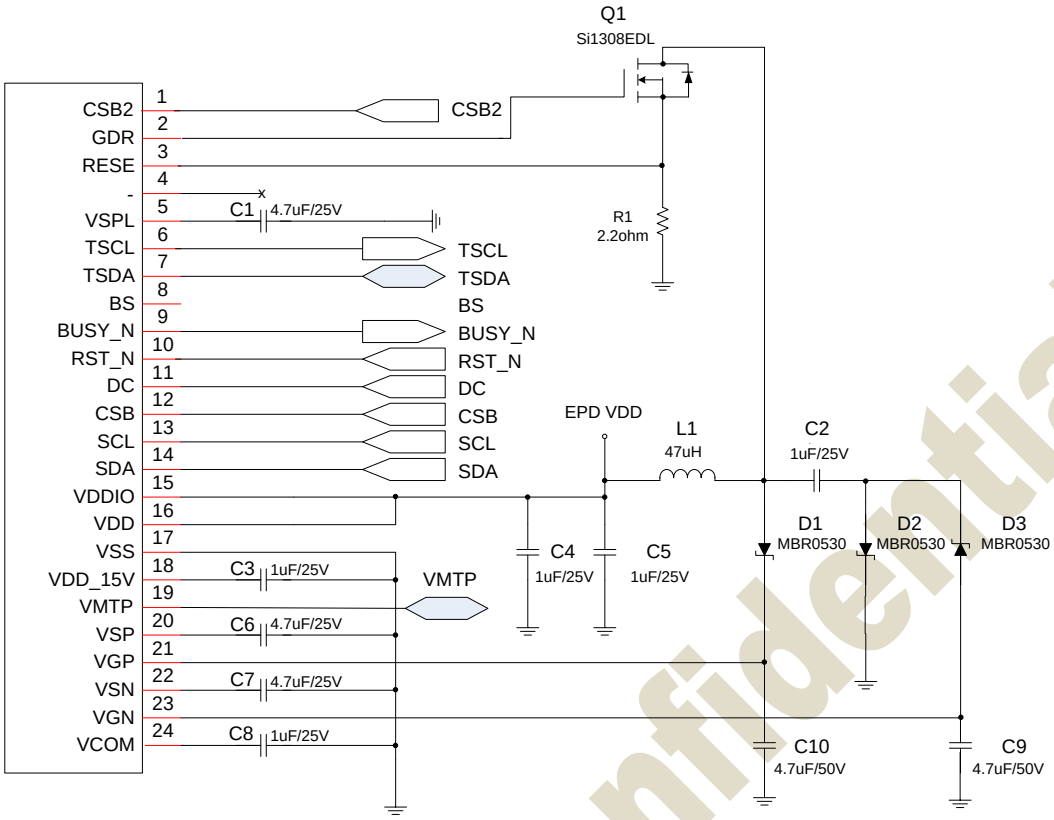
Normal type (TPS=High, P-Type TFT)

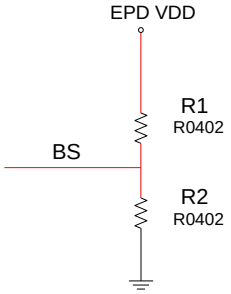


Cascade type



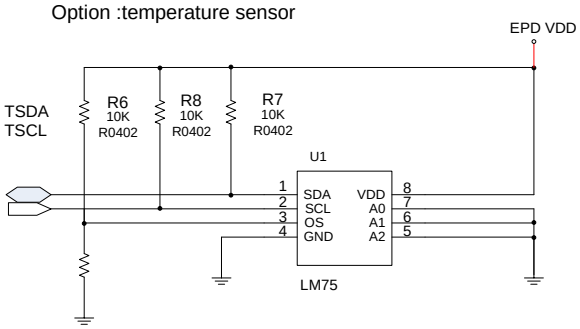
4. APPLICATION CIRCUIT





	R1	R2
3- wire SPI (CSB, SDA, SCL)	10K	NC
4-wire SPI (DC, CSB, SDA, SCL)	NC	10K

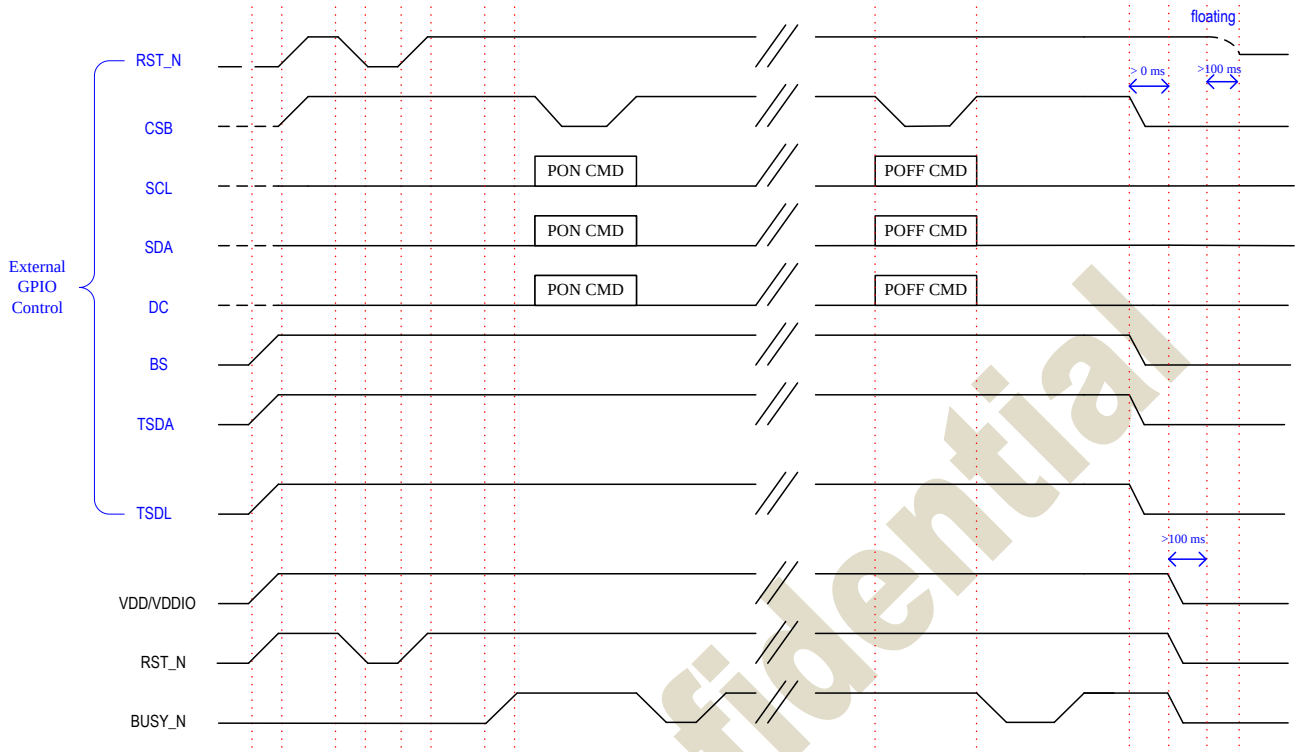
Option :temperature sensor



Reference table of the device:

Device no.	Value	Reference
C2,C3,C4,C5,C8	1uF	0603, X5R/X7R, voltage rating : 25V
C1,C6,C7	4.7uF	0603, X5R/X7R, voltage rating : 25V
C9,C10	4.7uF	0603, X5R/X7R, voltage rating : 50V
R1	2.2Ω	0603, +/-1% variation
Q1	NMOS	Si1308EDL、Si1304BDL - Drain-source break volatage≧30V - Gate-source threshold voltage≦1.5V - Drain-source on-state resistance<400mΩ
L1	47uH	NR4018T470M、CDRH2D18/LDNP-470NC - Fixed - Maximum DC current~420mA - Maximum DC resistance~650mΩ
D1~D3	Diode	MBR0530 - Reverse DC voltage≧30V - Forward current≧500mA - Forward voltage≦430mV

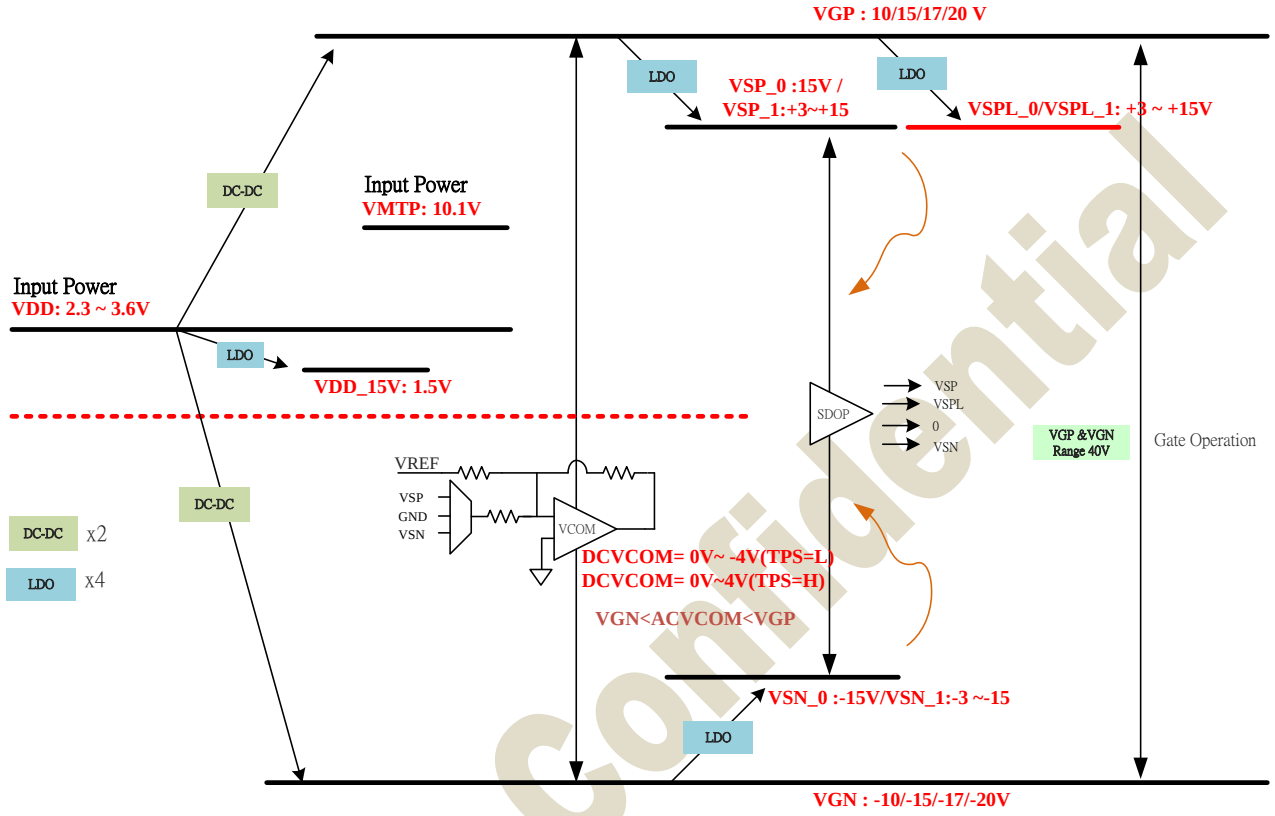
4.1 External GPIO Control



Note:
TSDA: I^2C data for external temperature sensor
TSCL: I^2C clock for external temperature sensor
(I^2C interface need external pull high resistance. Pull low or floating If not used.)

5. APPLICATION POWER CIRCUIT

5.1 Power Generation



6. PIN DESCRIPTION

6.1 Pin define

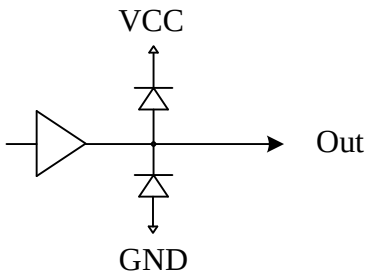
Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 5	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 5	Serial communication clock input.
DC	I	Type 5	Serial communication Command/Data input L: Command H: data Connect to VDD if BS=High.
Control Interface			
RST_N	I	Type 2	Global reset pin. Low reset. (normal pull high) When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will be released to floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= ”0” : Driver is busy, data/VCOM is transforming. BUSY_N= ”1” : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF
TSCL	I/O	Type 4	I^2C clock for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used. (Default low)
TSDA	I/O	Type 4	I^2C data for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used.(Default low)
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
TPS	I	Type 5	Panel TFT polarity selection Low: N-type High:P-type Must pull high or low
Output Driver			
S[799:0]	O	-	Source driver output signals.
G[599:0]	O	-	Gate driver output signals..
Border			
VBD[2:1]	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (VCM_DC) V 2. (15 + VCM_DC) V or (-15 + VCM_DC) V 3. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.
FB	P	-	Keep open
VGP	P		Positive gate voltage

Pin Name	Pin Type	I/O Structure	Description
VGN	P	-	Negative gate voltage.
VSP	P	-	Positive source voltage
VSN	P	-	Negative source voltage.
VSPL	P	-	Positive source voltage
Power Supply			
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power.
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_15V	P	-	1.5V voltage input &output
VMTP	P	-	MTP program power (10.1V)
Reserved Pins			
T_N18V	I/O	-	Test pin.Leave open or pull gnd.
T_LDON5V	I/O	-	Test pin.Leave open or pull gnd.
T_VCOM	I/O	-	Test pin.Leave open or pull gnd.
T_VSPD_REF	I/O	-	Test pin.Leave open or pull gnd.
T_IBIAS	I/O	-	Test pin.Leave open or pull gnd.
T_VREF	I/O	-	Test pin.Leave open or pull gnd.
T_EN_LSH	I/O	-	Test pin.Leave open or pull gnd.
T_VTSEN	I/O	-	Test pin.Leave open or pull gnd.
T_SAR_REF	I/O	-	Test pin.Leave open or pull gnd.
T_IN[2:0]	I/O	-	Test pin.Leave open or pull gnd.
T_DEBUG[8:0]	I/O	-	Test pin.Leave open or pull gnd.
T_EX_SYSCLK	I/O	-	Test pin.Leave open or pull gnd.
T_EX_REFCLK	I/O	-	Test pin.Leave open or pull gnd.
T_EN_DIG	I/O	-	Test pin.Leave open or pull gnd.
SyncD	I/O	Type 4	Cascade data signal. Leave open or pull gnd if it is not used.
SyncE	I/O	Type 4	Cascade data2 signal. Leave open or pull gnd if it is not used.
SyncC	I/O	Type 4	Cascade clock signal. Leave open or pull gnd if it is not used.
PckI	I	Type 3	Break panel check input. Leave open or gnd if it is not used.
PckO	O	Type 1	Break panel check output. Leave open or gnd if it is not used.
DUMMY[91:0]	D	-	Dummy pin. Leave open or pull gnd.

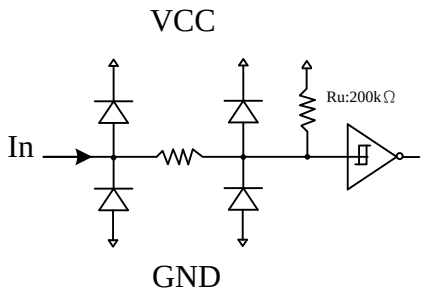
Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6.2 I/O Pin Structure

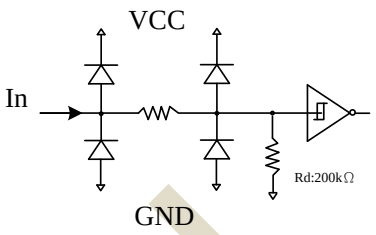
Type 1



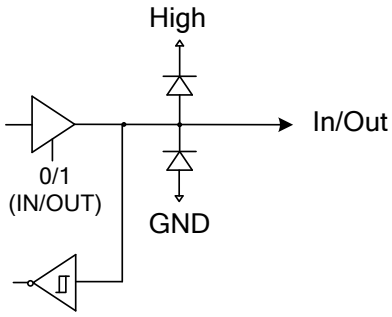
Type 2



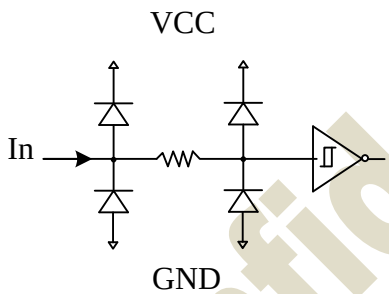
Type 3



Type 4



Type 5



6.3 Value of wiring resistance to each pin

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VCOM	5ohm	TSDA	100ohm
VGP	5ohm	TSCL	100ohm
VGN	5ohm	BS	100ohm
VSP	5ohm	RESE	5ohm
VSN	5ohm	GDR	5ohm
VSPL	5ohm	SDA	100ohm
VMTP	5ohm	SCL	100ohm
VDD_15V	5ohm	CSB	100ohm
VSSA	5ohm	DC	100ohm
VDDIO	5ohm	RST_N	100ohm
VSS	5ohm	SyncD	100ohm
VDDP	5ohm	SyncE	100ohm
VDD	5ohm	SyncC	100ohm
MS	100ohm	PCKI	100ohm
Test pin	100ohm	PCKO	100ohm
BUSY_N	100ohm	TPS	100ohm

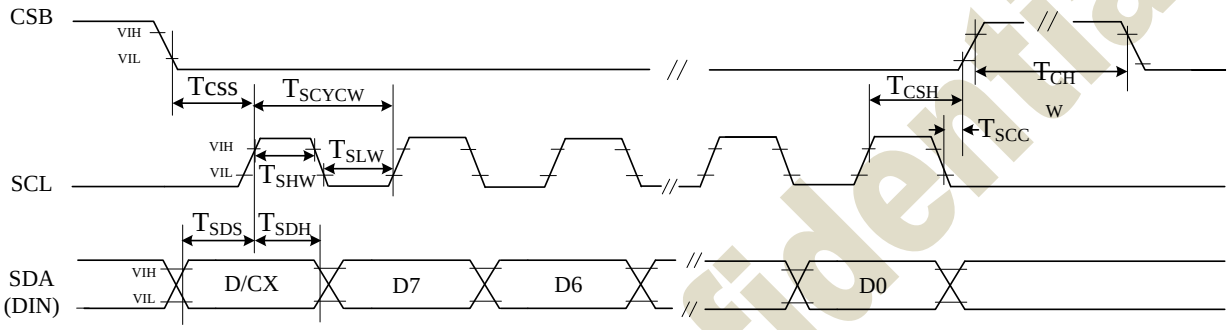
7. SPI COMMAND DESCRIPTION

JD79665 use the 3-wire/4-wire serial port as communication interface for all the function and command setting.

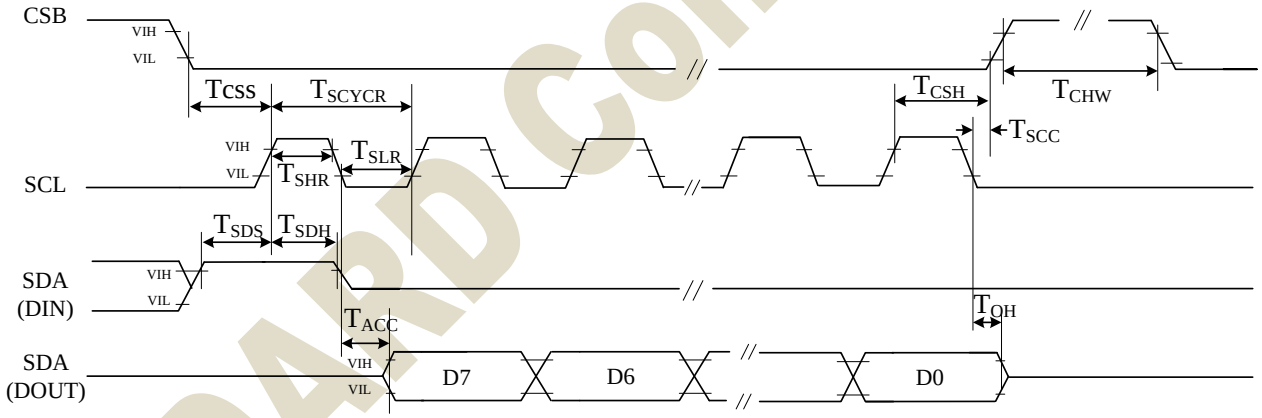
JD79665 3-wire/4-wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

Under read mode, 3-wire/4-wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-wire/4-wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

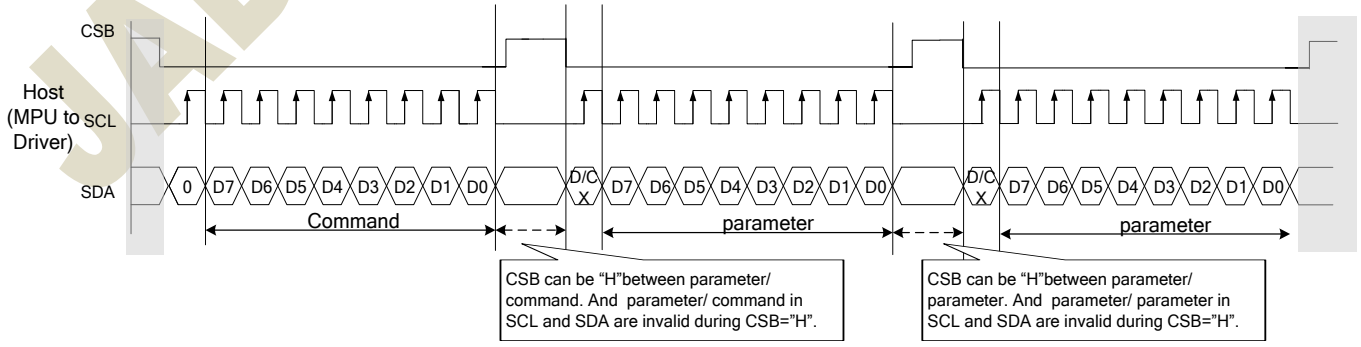
7.1 “3-Wire” Serial Port Interface



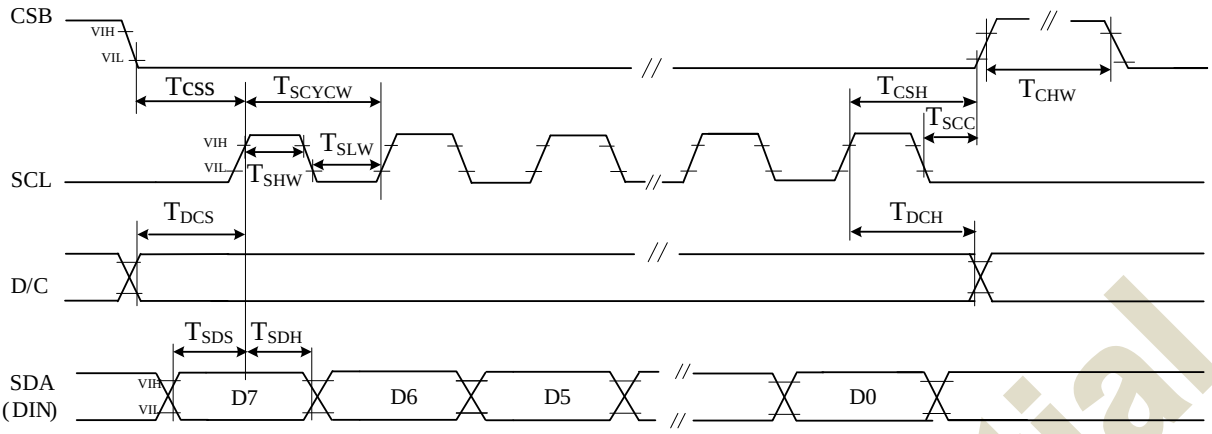
3 pin serial interface characteristics (write mode)



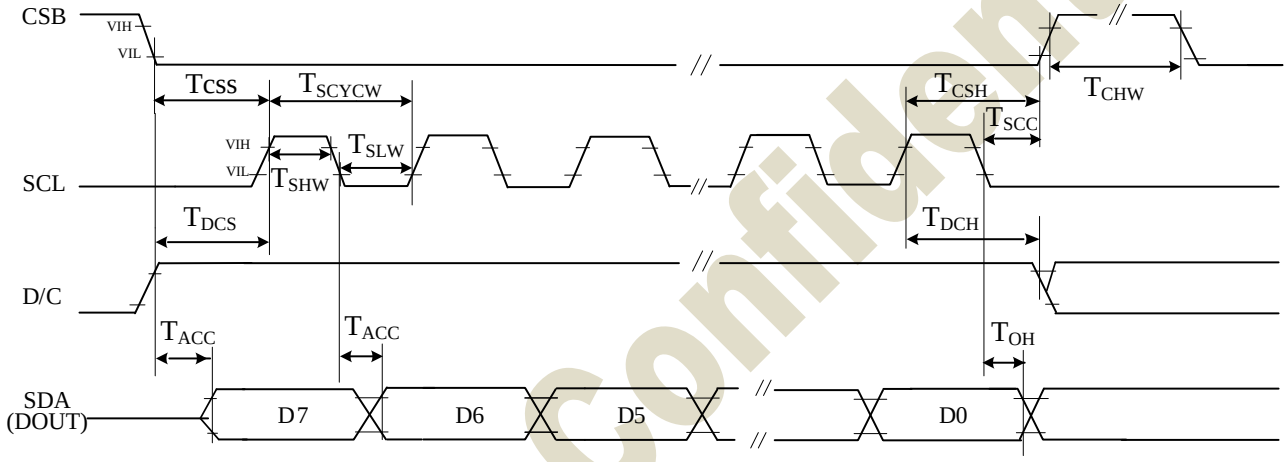
3 pin serial interface characteristics (read mode)



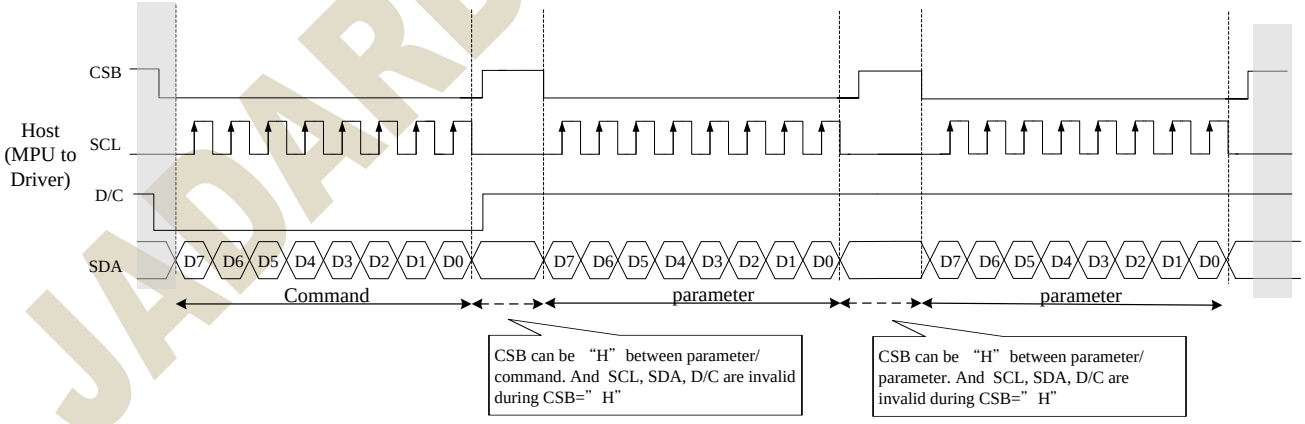
7.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)



8. SPI CONTROL REGISTERS:

8.1 Register Table

Following table list all the SPI control registers and bit name definition for JD79665. Refer to the next section for detail register function description.

Address	command			Bit								
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
		W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	BD_EN	-	-	VSC_EN	VDS_EN	VDG_EN	07h
		W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
		W	1	-	VSPL_0[6]	VSPL_0[5]	VSPL_0[4]	VSPL_0[3]	VSPL_0[2]	VSPL_0[1]	VSPL_0[0]	00h
		W	1	-	VSP_1[6]	VSP_1 [5]	VSP_1 [4]	VSP_1 [3]	VSP_1 [2]	VSP_1 [1]	VSP_1 [0]	00h
		W	1	-	VSN_1[6]	VSN_1[5]	VSN_1[4]	VSN_1[3]	VSN_1[2]	VSN_1[1]	VSN_1[0]	00h
		W	1	-	VSPL_1[6]	VSPL_1[5]	VSPL_1[4]	VSPL_1[3]	VSPL_1[2]	VSPL_1[1]	VSPL_1[0]	00h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
		W	1	-	-	-	-	-	-	-	-	00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00h
		W	1	-	-	PHA_ON[5:0]						02h
		W	1	-	-	PHA_OFF[5:0]						07h
		W	1	-	-	PHB_ON[5:0]						02h
		W	1	-	-	PHB_OFF[5:0]						07h
		W	1	-	-	PHC_ON[5:0]						02h
		W	1	-	-	PHC_OFF[5:0]						07h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission (DTM)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
		W	1	-	-	-	-	-	-	-	-	00H
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	-	-	-	Dyna	FR[2:0]			02h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[7]	D8/TS[6]	D7/TS[5]	D6/TS[4]	D5/TS[3]	D4/TS[2]	D3/TS[1]	--
		R	1	D2/ TS[9]	D1/TS[8]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	--

R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[2]	VBD[1]	VBD[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	--
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R65H	Gate/Source Start Setting(GSST)	W	0	0	1	1	0	0	1	0	1	65H
		W	1	-	-	-	-	-	-	S_start(9)	S_start(8)	00h
		W	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00h
		W	1	-	-	-	-	-	-	G_start(9)	G_start(8)	00h
		W	1	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	0	0	0	0	1	1	1	0	0Eh
		R	1	0	0	0	0	0	0	1	0	02h
		R	1	0	0	0	0	0	0	0	1	01h
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h
R83H	Partial Window (PTLW)	W	0	1	0	0	0	0	0	1	1	83H
		W	1	-	-	-	PTH_ENB	-	-	HRST(9)	HRST(8)	00h
		W	1	HRST(7)	HRST(6)	HRST(5)	HRST(4)	HRST(3)	HRST(2)	0	0	00h
		W	1	-	-	-	-	-	-	HRED(9)	HRED(8)	00h
		W	1	HRED(7)	HRED(6)	HRED(5)	HRED(4)	HRED(3)	HRED(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	-	PMODE	00h
R90H	Program mode(PGM)	W	0	1	0	0	1	0	0	0	0	90H
R91H	Active Program(APG)	W	0	1	0	0	1	0	0	0	1	91H
R92H	Read MTP data (RMTP)	W	0	1	0	0	1	0	0	1	0	92H
		R	1	#	#	#	#	#	#	#	#	-
RA2H	MTP Program Config Register(PGM_CFG)	W	0	1	0	1	0	0	0	1	0	A2H
		W	1	-	-	-	VMTPSEL	-	-	M_dis	S_dis	00h
		W	1	PGM_SADDR[15:8]								00h
		W	1	PGM_SADDR[7:0]								00h
		W	1	PGM_DSIZE[15:8]								0Fh
		W	1	PGM_DSIZE[7:0]								00h
RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H
		W	1	-	-	-	-	-	-	-	CCEIN	00h
RE3H	Power saving(PWS)	W	0	1	1	1	0	0	0	1	1	E3H
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00h
		W	1		GD_WR2]	GD_WR[1]	GD_WR[0]		GD_WF[2]	GD_WF[1]	GD_WF[0]	00h
RE4H	LVD voltage Select(LVSEL)	W	0	1	1	1	0	0	1	0	0	E4H
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h

8.2 Register Description

R/W: 0:Write Cycle 1:Read Cycle
D/CX:0:Command/1:Data
D7~D0:-:Don't Care

8.2.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st parameter

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and Source / Border / Vcom are kept 0V or floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →…→S2→Last data=S1. 1: Shift right: First data=S1→S2 →…→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→G2→Last line=G1. 1:Scan up; First line=G1→G2 →…→Gn-1→Last line=Gn. (default)
5	PST_MODE	Power switch operation mode 0:Power switching time in the period of frame scanning.(default) 1:Power switching time in the external period before frame scanning.
7-6	RES[1,0]	Resolution setting 00: Display resolution is 800x600(default) 01: Display resolution is 720x540 10: Display resolution is 640x480 11: Display resolution is 600x448

2nd parameter

Bit	Name	Description
0	VC_LUTZ	VCOM status function 0 : No effect 1 : After refreshing display, the output of VCOM is set to floating automatically (default)
1	NORG	VCOM status function 0 : No effect (default) 1 : After refreshing display, VCOM is tied to GND before power off
2	TIEG	VGN power off status function 0 : No effect (default) 1 : Power off, VGN will be tied to GND
3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling booster,Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high,Temperature Sensor will be activated automatically one time. (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	FOPT	FOPT function 0: Scan 1 frame after waveform finished(default) 1: No scan after waveform finished and switch the source channel output to Hiz.
7	LUT_EN	LUT selection setting 0 : Using LUT from MTP(default) 1 : Using LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.
FOPT: Power off floating.

Notes:
1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Dummy source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off.SD output and VCOM will base on previous condition. It may have two condition:0V or floating.
4. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. Source/Gate/Border/VCOM will be released to floating

Restriction	

8.2.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	BD_EN	-	-	VSC_EN	VDS_EN	VDG_EN	07h
2nd Parameter	W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
3rd Parameter	W	1	-	VSPL_0 [6:0]							00h
4th Parameter	W	1	-	VSP_1 [6:0]							00h
5th Parameter	W	1	-	VSN_1 [6:0]							00h
6th Parameter	W	1	-	VSPL_1 [6:0]							00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	Gate power selection. 0 : External gate power from VGP/VGN pins. 1 : Internal DCDC function for generate VGP/VGN. (default)
1	VDS_EN	Source power selection. 0 : External source power from VSP/VSN pins. 1 : Internal regulator function for generate VSP/VSN (default)
2	VSC_EN	Source LV power selection. 0 : External source power from VSPL pins. 1 : Internal regulator function for generate VSPL (default)

5	BD_EN	**Border LDO enable** (when TPS=LOW) 0:Border LDO disable(default)

code	Border level selection
00	VCOM
01	VSP
10	VSN
11	VSPL

1:Border LDO enable

code	Border level selection
00	VCOM
01	VSP+VCOM
10	VSN+VCOM
11	VSPL+VCOM

Border LDO enable (when TPS=HIGH)
0:Border LDO disable(default)

code	Border level selection
00	VCOM
01	VSP
10	VSN
11	VSPL

1:Border LDO enable

code	Border level selection
00	VCOM
01	VSP+VCOM
10	VSN+VCOM
11	VSPL+VCOM

2nd Parameter:

Bit	Name	Description
1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v

3rd & 4th & 6th Parameter: Internal VSP_1/VSPL_0/ VSPL_1 power selection

Bit	Name	Description
6-0	VSP_1 & VSPL_0 & VSPL_1	**Internal VSP & VSPL power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	3	0101001	29h	7.1	1010010	52h	11.2
0000001	01h	3.1	0101010	2Ah	7.2	1010011	53h	11.3
0000010	02h	3.2	0101011	2Bh	7.3	1010100	54h	11.4
0000011	03h	3.3	0101100	2Ch	7.4	1010101	55h	11.5
0000100	04h	3.4	0101101	2Dh	7.5	1010110	56h	11.6
0000101	05h	3.5	0101110	2Eh	7.6	1010111	57h	11.7
0000110	06h	3.6	0101111	2Fh	7.7	1011000	58h	11.8
0000111	07h	3.7	0110000	30h	7.8	1011001	59h	11.9
0001000	08h	3.8	0110001	31h	7.9	1011010	5Ah	12
0001001	09h	3.9	0110010	32h	8	1011011	5Bh	12.1
0001010	0Ah	4	0110011	33h	8.1	1011100	5Ch	12.2
0001011	0Bh	4.1	0110100	34h	8.2	1011101	5Dh	12.3
0001100	0Ch	4.2	0110101	35h	8.3	1011110	5Eh	12.4
0001101	0Dh	4.3	0110110	36h	8.4	1011111	5Fh	12.5
0001110	0Eh	4.4	0110111	37h	8.5	1100000	60h	12.6
0001111	0Fh	4.5	0111000	38h	8.6	1100001	61h	12.7
0010000	10h	4.6	0111001	39h	8.7	1100010	62h	12.8
0010001	11h	4.7	0111010	3Ah	8.8	1100011	63h	12.9
0010010	12h	4.8	0111011	3Bh	8.9	1100100	64h	13
0010011	13h	4.9	0111100	3Ch	9	1100101	65h	13.1
0010100	14h	5	0111101	3Dh	9.1	1100110	66h	13.2
0010101	15h	5.1	0111110	3Eh	9.2	1100111	67h	13.3
0010110	16h	5.2	0111111	3Fh	9.3	1101000	68h	13.4
0010111	17h	5.3	1000000	40h	9.4	1101001	69h	13.5
0011000	18h	5.4	1000001	41h	9.5	1101010	6Ah	13.6
0011001	19h	5.5	1000010	42h	9.6	1101011	6Bh	13.7
0011010	1Ah	5.6	1000011	43h	9.7	1101100	6Ch	13.8
0011011	1Bh	5.7	1000100	44h	9.8	1101101	6Dh	13.9
0011100	1Ch	5.8	1000101	45h	9.9	1101110	6Eh	14
0011101	1Dh	5.9	1000110	46h	10	1101111	6Fh	14.1
0011110	1Eh	6	1000111	47h	10.1	1110000	70h	14.2
0011111	1Fh	6.1	1001000	48h	10.2	1110001	71h	14.3
0100000	20h	6.2	1001001	49h	10.3	1110010	72h	14.4
0100001	21h	6.3	1001010	4Ah	10.4	1110011	73h	14.5
0100010	22h	6.4	1001011	4Bh	10.5	1110100	74h	14.6
0100011	23h	6.5	1001100	4Ch	10.6	1110101	75h	14.7
0100100	24h	6.6	1001101	4Dh	10.7	1110110	76h	14.8
0100101	25h	6.7	1001110	4Eh	10.8	1110111	77h	14.9
0100110	26h	6.8	1001111	4Fh	10.9	1111000	78h	15
0100111	27h	6.9	1010000	50h	11	other		15
0101000	28h	7	1010001	51h	11.1			

5th Parameter: Internal VSN_1 power selection

Bit	Name	Description
6-0	VSN_1	**Internal VSN power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	-3	0101001	29h	-7.1	1010010	52h	-11.2
0000001	01h	-3.1	0101010	2Ah	-7.2	1010011	53h	-11.3
0000010	02h	-3.2	0101011	2Bh	-7.3	1010100	54h	-11.4
0000011	03h	-3.3	0101100	2Ch	-7.4	1010101	55h	-11.5
0000100	04h	-3.4	0101101	2Dh	-7.5	1010110	56h	-11.6
0000101	05h	-3.5	0101110	2Eh	-7.6	1010111	57h	-11.7
0000110	06h	-3.6	0101111	2Fh	-7.7	1011000	58h	-11.8
0000111	07h	-3.7	0110000	30h	-7.8	1011001	59h	-11.9
0001000	08h	-3.8	0110001	31h	-7.9	1011010	5Ah	-12
0001001	09h	-3.9	0110010	32h	-8	1011011	5Bh	-12.1
0001010	0Ah	-4	0110011	33h	-8.1	1011100	5Ch	-12.2
0001011	0Bh	-4.1	0110100	34h	-8.2	1011101	5Dh	-12.3
0001100	0Ch	-4.2	0110101	35h	-8.3	1011110	5Eh	-12.4
0001101	0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh	-12.5
0001110	0Eh	-4.4	0110111	37h	-8.5	1100000	60h	-12.6
0001111	0Fh	-4.5	0111000	38h	-8.6	1100001	61h	-12.7
0010000	10h	-4.6	0111001	39h	-8.7	1100010	62h	-12.8
0010001	11h	-4.7	0111010	3Ah	-8.8	1100011	63h	-12.9
0010010	12h	-4.8	0111011	3Bh	-8.9	1100100	64h	-13
0010011	13h	-4.9	0111100	3Ch	-9	1100101	65h	-13.1
0010100	14h	-5	0111101	3Dh	-9.1	1100110	66h	-13.2
0010101	15h	-5.1	0111110	3Eh	-9.2	1100111	67h	-13.3
0010110	16h	-5.2	0111111	3Fh	-9.3	1101000	68h	-13.4
0010111	17h	-5.3	1000000	40h	-9.4	1101001	69h	-13.5
0011000	18h	-5.4	1000001	41h	-9.5	1101010	6Ah	-13.6
0011001	19h	-5.5	1000010	42h	-9.6	1101011	6Bh	-13.7
0011010	1Ah	-5.6	1000011	43h	-9.7	1101100	6Ch	-13.8
0011011	1Bh	-5.7	1000100	44h	-9.8	1101101	6Dh	-13.9
0011100	1Ch	-5.8	1000101	45h	-9.9	1101110	6Eh	-14
0011101	1Dh	-5.9	1000110	46h	-10	1101111	6Fh	-14.1
0011110	1Eh	-6	1000111	47h	-10.1	1110000	70h	-14.2
0011111	1Fh	-6.1	1001000	48h	-10.2	1110001	71h	-14.3
0100000	20h	-6.2	1001001	49h	-10.3	1110010	72h	-14.4
0100001	21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5
0100010	22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6
0100011	23h	-6.5	1001100	4Ch	-10.6	1110101	75h	-14.7
0100100	24h	-6.6	1001101	4Dh	-10.7	1110110	76h	-14.8
0100101	25h	-6.7	1001110	4Eh	-10.8	1110111	77h	-14.9
0100110	26h	-6.8	1001111	4Fh	-10.9	1111000	78h	-15
0100111	27h	-6.9	1010000	50h	-11	other		-15
0101000	28h	-7	1010001	51h	-7.1			

Notes:

1. VSP_0/VSN_0 voltage output is ±15 V fixed value.
2. When switching Mode0 or Mode1,the voltage output is:
   Mode0: VSP_0(+15) / VSN_0 (-15) / VSPL_0 (+3~+15)
   Mode1: VSP_1(+3 ~ +15) / VSN_1(-3 ~ -15) / VSPL_1(+3 ~ +15)

	Mode0	Mode1
VSP	VSP_0(+15)	VSP_1(+3~+15)
VSN	VSN_0(-15)	VSN_1(-3~-15)
VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)

3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows
   I. VGP- VSP_0 / VSPL_0 / VSP_1 / VSPL_1 >= 2v
   II. VGN- VSN_0 / VSN_1 >= -2v
   For example:

	symbol	Voltage setting	Real Voltage
Voltage	VGP	+10v	+10v
	VGN	-10v	-10v
	VSP_0	+15v	+8v
	VSN_0	-15v	-8v
	VSP_1	+5v	+5v
	VSN_1	-5v	-5v
	VSPL	+15v	+8v
	VCOMH	+15v+(-2v)	+8v +(-2v)
	VCOML	-15v+(-2v)	-8v +(-2v)
	VCOMDC	-2v	-2v

4. Voltage setting limit: VSP_0 ≥ VSPL_0 , VSP_1 ≥ VSPL_1

Restriction	

8.2.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H
1st Parameter	W	0	-	-	-	-	-	-	-	-	00

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R02h = 0x00h ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

8.2.4R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence (base on PWR command), BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

8.2.5 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	-	-	-	-	PHB_SFT [1:0]		PHA_SFT [1:0]		00h
2nd Parameter	W	1	-	-	PHA_ON [5:0]						02h
3rd Parameter	W	1	-	-	PHA_OFF [5:0]						07h
4th Parameter	W	1	-	-	PHB_ON [5:0]						02h
5th Parameter	W	1	-	-	PHB_OFF [5:0]						07h
6th Parameter	W	1	-	-	PHC_ON [5:0]						02h
7th Parameter	W	1	-	-	PHC_OFF [5:0]						07h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
1-0	PHA_SFT	Soft start period of phase A: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS
3-2	PHB_SFT	Soft start period of phase B: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Driving strength of PHA_ON & PHB_ON & PHC_ON	000000	strength1	010110	strength23	101100	strength45
	000001	strength2	010111	strength24	101101	strength46
	000010	strength3	011000	strength25	101110	strength47
	000011	strength4	011001	strength26	101111	strength48
	000100	strength5	011010	strength27	110000	strength49
	000101	strength6	011011	strength28	110001	strength50
	000110	strength7	011100	strength29	110010	strength51
	000111	strength8	011101	strength30	110011	strength52
	001000	strength9	011110	strength31	110100	strength53
	001001	strength10	011111	strength32	110101	strength54
	001010	strength11	100000	strength33	110110	strength55
	001011	strength12	100001	strength34	110111	strength56
	001100	strength13	100010	strength35	111000	strength57
	001101	strength14	100011	strength36	111001	strength58
	001110	strength15	100100	strength37	111010	strength59
	001111	strength16	100101	strength38	111011	strength60
	010000	strength17	100110	strength39	111100	strength61
	010001	strength18	100111	strength40	111101	strength62
	010010	strength19	101000	strength41	111110	strength63
	010011	strength20	101001	strength42	111111	strength64
	010100	strength21	101010	strength43		
	010101	strength22	101011	strength44		

Description

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Minimum OFF time setting of PHA_OFF & PHB_OFF & PHC_OFF	000000	Period1	010110	Period23	101100	Period45
	000001	Period2	010111	Period24	101101	Period46
	000010	Period3	011000	Period25	101110	Period47
	000011	Period4	011001	Period26	101111	Period48
	000100	Period5	011010	Period27	110000	Period49
	000101	Period6	011011	Period28	110001	Period50
	000110	Period7	011100	Period29	110010	Period51
	000111	Period8	011101	Period30	110011	Period52
	001000	Period9	011110	Period31	110100	Period53
	001001	Period10	011111	Period32	110101	Period54
	001010	Period11	100000	Period33	110110	Period55
	001011	Period12	100001	Period34	110111	Period56
	001100	Period13	100010	Period35	111000	Period57
	001101	Period14	100011	Period36	111001	Period58
	001110	Period15	100100	Period37	111010	Period59
	001111	Period16	100101	Period38	111011	Period60
	010000	Period17	100110	Period39	111100	Period61
	010001	Period18	100111	Period40	111101	Period62
	010010	Period19	101000	Period41	111110	Period63
	010011	Period20	101001	Period42	111111	Period64
	010100	Period21	101010	Period43		
	010101	Period22	101011	Period44		

Restriction

8.2.6 R07H (DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

8.2.7 R10H (DTM): Data Start transmission Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM_master	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h
:	W	1	:		:		:		:		00h
Mth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 12H. Then chip will start to send data/VCOM for panel.

Pixel [1~n][1:0]: 2-bit/pixel

Image Data	DDX=1(default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00b	Gray0	ogray00	Gray3	ogray03
01b	Gray1	ogray01	Gray2	ogray02
10b	Gray2	ogray02	Gray1	ogray01
11b	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1,Pixel[1:0]=01 ->Gray level select=Gray1,follow LUT data output from IP output port"ogray01".

When DDX=0,Pixel[1:0]=11 ->Gray level select=Gray0,follow LUT data output from IP output port"ogray00"

Restriction

8.2.8 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

- While finished the data transmitting, user must send this command to driver and read Data_flag information.

1st Parameter:

Bit	Name	Description
7	Data_flag	0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.

After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.

Restriction

This command only actives when BUSY_N = "1".

8.2.9 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H
1st Parameter	W	1	-	-	-	-	-	-	-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R12H=0x00 While users send this command, driver will refresh display base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0"
Restriction	This command only actives when BUSY_N = "1"

8.2.10 R17H (AUTO): Auto Sequence

R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code(0xA5) = (PON→DRF→POF) AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)
Restriction	This command only actives when BUSY_N = "1".

8.2.11 R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	02h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

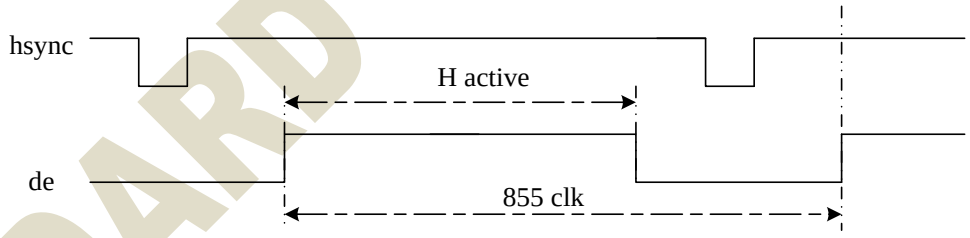
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

bit3	Dynamic frame rate
0	Disable(default)
1	Enable

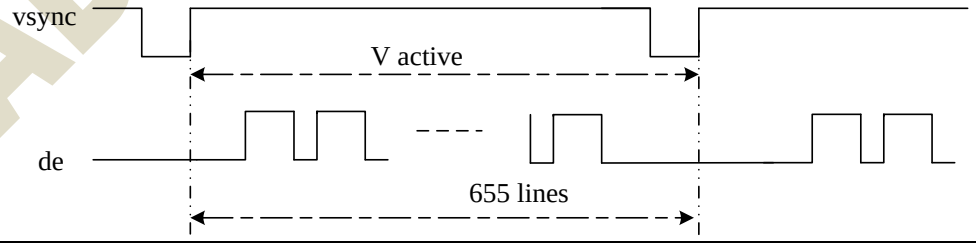
FR[2:0]	Frame rate
000	12.5 Hz
001	25 Hz
010	50 Hz(default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

remark

-Horizental



-Vertical



Restriction

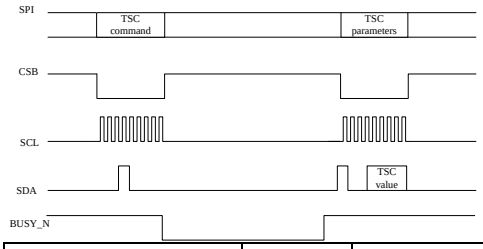
8.2.12 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2/ TS[9]	D1/ TS[8]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:
This command indicates the temperature value.
If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.
If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[9:8]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction: This command only actives when BUSY_N = "1".

8.2.13 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Name	Description
3-0	TO[3:0]	Temperature level: 0000: +0℃ (default) 0001: +0.5℃ 0010: +1℃ 0011: +1.5℃ 0100: +2℃ 0101: +2.5℃ 0110: +3℃ 0111: +3.5℃ 1000: -4℃ 1001: -3.5℃ 1010: -3℃ 1011: -2.5℃ 1100: -2℃ 1101: -1.5℃ 1110: -1℃ 1111: -0.5℃
4	TO[4]	0: +0.0℃ (default) 1: +0.25℃
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

Restriction: This command only actives after R04H(PON)

8.2.14 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	Name	Description
2-0	WATTR[2:0]	Pointer setting
5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)
7-6	WATTR[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	Name	Description
7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	Name	Description
7-0	WLSB[7:0]	LSByte of write-data to external temperature sensor

Restriction: This command only actives after R04H(PON)

8.2.15 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSR	W	0	0	1	0	0	0	0	1	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

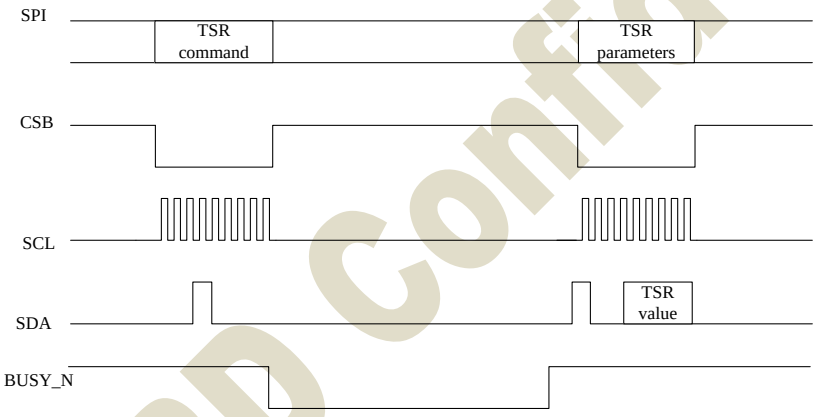
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	Name	Description
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	Name	Description
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor



Restriction: This command only actives after R04H(PON)

8.2.16 R50H (CDI): VCOM and DATA interval setting Register

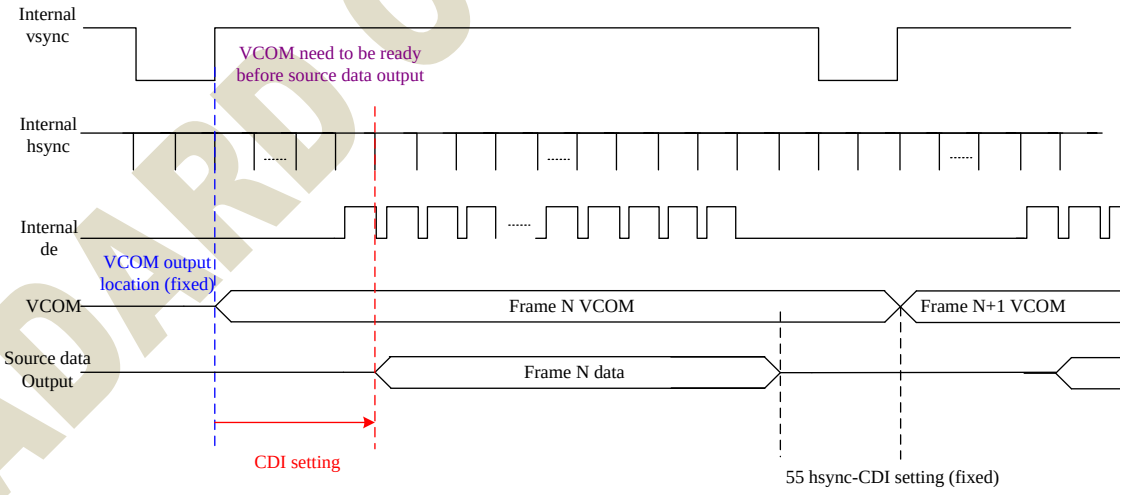
R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[2]	VBD[1]	VBD [0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command can set 2 kinds of parameters, 1.VCOM to data output interval(CDI)
:
CDI[3:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (55hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync(default) 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[2:0]: Border data selection. (from LUT output by IP port border_w[1:0])

This register will make boarder pin output being mapped to a certain gray scale.

Bit 4	Bit7-5	Description	IP setting for Border LUT select
DDX	VBD[2:0]	Gray level	
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating	N/A

Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V,without VCOM offset, the real output on Boarder pin shall be 15V.

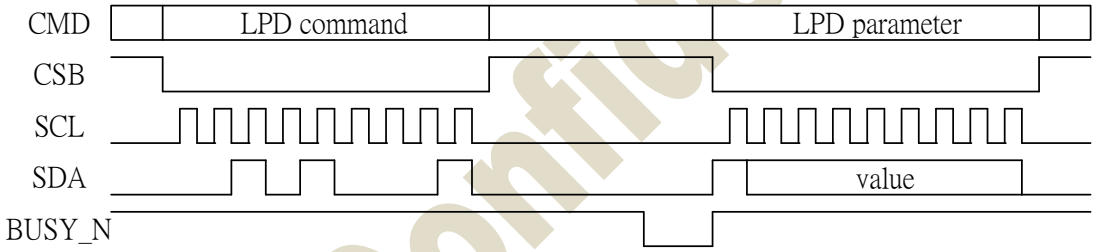
Boarder output will follow FOPT definition being defined in R00h.

Restriction	

8.2.17 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)). 1st Parameter: Bit 0 / LPD 0 / Low power input. 1 / Normal status. 
Restriction	This command only actives when BUSY_N = "1".

8.2.18 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
3th Parameter	W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES Note: No matter HRES[1:0] value being filled, it's always be 00b. Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[9:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:2]*4-1 EX :800X600 GD: First G active = G0 LAST active GD= 0+600-1= 599; (G599) SD : First active channel: =S0 LAST active SD=0+200*4-1=799; (S799)
Restriction	Horizontal resolution should be 4-multiple.

8.2.19 R65H (GSST): Gate/Source Start Setting Register

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1st Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2nd Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h
3rd Parameter	W	1	-	-	-	-	-	-	G_start[9]	G_start[8]	00h
4th Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: Note: No matterS_start [1:0] value being filled, it's always be 00 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line
Restriction	S_Start should be the multiple of 4

8.2.20 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	0	0	0	0	1	1	1	0	0Eh
2nd Parameter	R	1	0	0	0	0	0	0	1	0	02h
3rd Parameter	R	1	0	0	0	0	0	0	0	1	01h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: 1st & 2nd & 3rd Parameter:

Bit	Description
7-0	CHIP_REV

Restriction	

8.2.21 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h

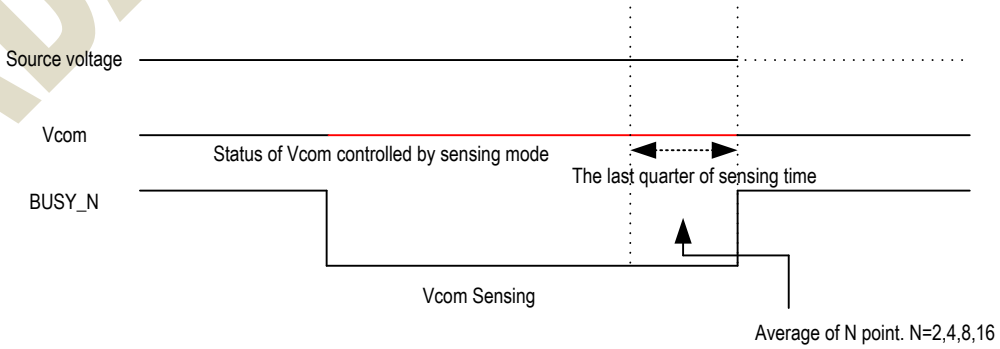
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSPL_0 during Auto Measure VCOM period.
3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 5s (default) 01: 10s 10: 15s 11: 20s
7-6	P[1:0]	The sensing points of sampling time 00: 2 (default) 01: 4 10: 8 11: 16 Sampling time = the last quarter of sensing time (T) VCOM = average of N points. N=2,4,8,16



Restriction: This command only actives when BUSY_N = "1".

8.2.22 R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter: (when TPS=LOW)

Bit	Name	Description
6-0	VV[6:0]	**VCOM value**

VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)
0000000	00h	0	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

1st Parameter: (when TPS=HIGH)

Bit	Name	Description
6-0	VV[6:0]	**VCOM value**

VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)
0000000	00h	0	0011100	1Ch	1.4	0111000	38h	2.8
0000001	01h	0.05	0011101	1Dh	1.45	0111001	39h	2.85
0000010	02h	0.1	0011110	1Eh	1.5	0111010	3Ah	2.9
0000011	03h	0.15	0011111	1Fh	1.55	0111011	3Bh	2.95
0000100	04h	0.2	0100000	20h	1.6	0111100	3Ch	3
0000101	05h	0.25	0100001	21h	1.65	0111101	3Dh	3.05
0000110	06h	0.3	0100010	22h	1.7	0111110	3Eh	3.1
0000111	07h	0.35	0100011	23h	1.75	0111111	3Fh	3.15
0001000	08h	0.4	0100100	24h	1.8	1000000	40h	3.2
0001001	09h	0.45	0100101	25h	1.85	1000001	41h	3.25
0001010	0Ah	0.5	0100110	26h	1.9	1000010	42h	3.3
0001011	0Bh	0.55	0100111	27h	1.95	1000011	43h	3.35
0001100	0Ch	0.6	0101000	28h	2	1000100	44h	3.4
0001101	0Dh	0.65	0101001	29h	2.05	1000101	45h	3.45
0001110	0Eh	0.7	0101010	2Ah	2.1	1000110	46h	3.5
0001111	0Fh	0.75	0101011	2Bh	2.15	1000111	47h	3.55
0010000	10h	0.8	0101100	2Ch	2.2	1001000	48h	3.6
0010001	11h	0.85	0101101	2Dh	2.25	1001001	49h	3.65
0010010	12h	0.9	0101110	2Eh	2.3	1001010	4Ah	3.7
0010011	13h	0.95	0101111	2Fh	2.35	1001011	4Bh	3.75
0010100	14h	1	0110000	30h	2.4	1001100	4Ch	3.8
0010101	15h	1.05	0110001	31h	2.45	1001101	4Dh	3.85
0010110	16h	1.1	0110010	32h	2.5	1001110	4Eh	3.9
0010111	17h	1.15	0110011	33h	2.55	1001111	4Fh	3.95
0011000	18h	1.2	0110100	34h	2.6	1010000	50h	4
0011001	19h	1.25	0110101	35h	2.65	other	4	
0011010	1Ah	1.3	0110110	36h	2.7			
0011011	1Bh	1.35	0110111	37h	2.75			

Restriction	

8.2.23 R82H (VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	VDCS[6]	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.

1st Parameter: (when TPS=LOW)

Bit	Name	Description
6-0	VDCS[6:0]	**VCOM value**

VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)
0000000	00h	0(default)	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

1st Parameter: (when TPS=HIGH)

Bit	Name	Description
6-0	VDCS[6:0]	**VCOM value**

VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)
0000000	00h	0(default)	0011100	1Ch	1.4	0111000	38h	2.8
0000001	01h	0.05	0011101	1Dh	1.45	0111001	39h	2.85
0000010	02h	0.1	0011110	1Eh	1.5	0111010	3Ah	2.9
0000011	03h	0.15	0011111	1Fh	1.55	0111011	3Bh	2.95
0000100	04h	0.2	0100000	20h	1.6	0111100	3Ch	3
0000101	05h	0.25	0100001	21h	1.65	0111101	3Dh	3.05
0000110	06h	0.3	0100010	22h	1.7	0111110	3Eh	3.1
0000111	07h	0.35	0100011	23h	1.75	0111111	3Fh	3.15
0001000	08h	0.4	0100100	24h	1.8	1000000	40h	3.2
0001001	09h	0.45	0100101	25h	1.85	1000001	41h	3.25
0001010	0Ah	0.5	0100110	26h	1.9	1000010	42h	3.3
0001011	0Bh	0.55	0100111	27h	1.95	1000011	43h	3.35
0001100	0Ch	0.6	0101000	28h	2	1000100	44h	3.4
0001101	0Dh	0.65	0101001	29h	2.05	1000101	45h	3.45
0001110	0Eh	0.7	0101010	2Ah	2.1	1000110	46h	3.5
0001111	0Fh	0.75	0101011	2Bh	2.15	1000111	47h	3.55
0010000	10h	0.8	0101100	2Ch	2.2	1001000	48h	3.6
0010001	11h	0.85	0101101	2Dh	2.25	1001001	49h	3.65
0010010	12h	0.9	0101110	2Eh	2.3	1001010	4Ah	3.7
0010011	13h	0.95	0101111	2Fh	2.35	1001011	4Bh	3.75
0010100	14h	1	0110000	30h	2.4	1001100	4Ch	3.8
0010101	15h	1.05	0110001	31h	2.45	1001101	4Dh	3.85
0010110	16h	1.1	0110010	32h	2.5	1001110	4Eh	3.9
0010111	17h	1.15	0110011	33h	2.55	1001111	4Fh	3.95
0011000	18h	1.2	0110100	34h	2.6	1010000	50h	4
0011001	19h	1.25	0110101	35h	2.65	other		4
0011010	1Ah	1.3	0110110	36h	2.7			
0011011	1Bh	1.35	0110111	37h	2.75			

Restriction	

8.2.24 R83H (PTL): Partial Window Register

R83H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1st Parameter	W	1	-	-	-	PTH_ENB	-	-	HRST[9]	HRST[8]	00h
2nd Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	-	-	00h
3rd Parameter	W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4th Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	-	-	00h
5th Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
6th Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
7th Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
8th Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
9th Parameter	W	1	-	-	-	-	-	-	-	PMODE	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command sets partial window.

Name	Description
HRST[9:2]	Horizontal start address
HRED[9:2]	Horizontal end address. HRED must be greater than HRST.
VRST[9:0]	Vertical start address.
VRED[9:0]	Vertical end address. VRED must be greater than VRST.
PMODE	0: disable partial mode(default) 1: enable partial mode
PTH_ENB	0:Source output enable follow HRST and HRED 1:Source output disable

Note:
No matter HRST[1:0] value being filled, it's always be 00b.
No matter HRED[1:0] value being filled, it's always be 11b.

Gates scan both inside and outside of the partial window.

Restriction

8.2.25 R90H (PGM): Program Mode

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	0	1	0	0	0	0	90H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	

8.2.26 R91H (APG): Active Program

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

8.2.27 R92H (RMTP): Read MTP Data

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMTP	W	0	1	0	0	1	0	0	1	0	92H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the MTP								-
3rd Parameter	R	1	The data of address 0x001 in the MTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the MTP								-
6th~(m-1)th Parameter	R	1	…..								-
mth Parameter	R	1	The data of address (n) in the MTP								-

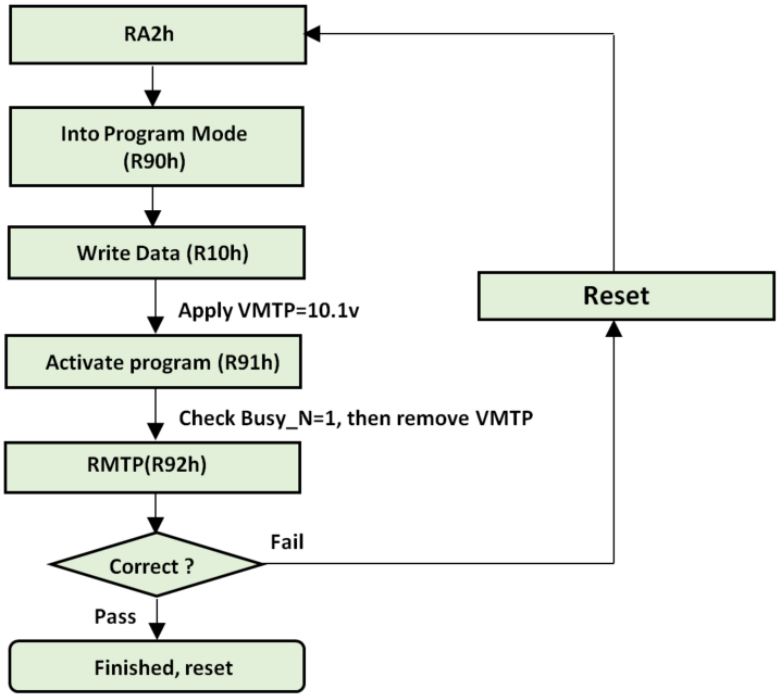
NOTE: "-" Don't care, can be set to VDD or GND level

Description

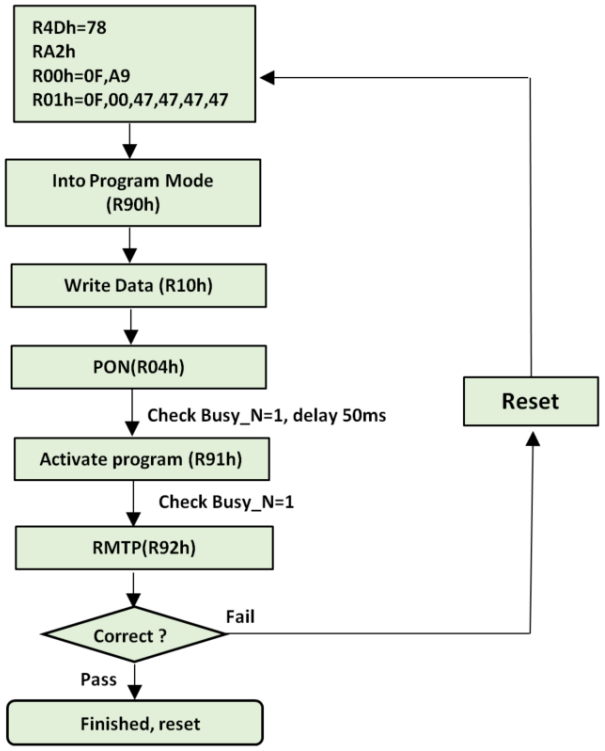
The command define as follows:

-The command is used for reading the content of MTP for checking the data of programming,

-The value of (n) is depending on the amount of programmed data, the max address= 0xFFF



The sequence of programming MTP(External power)



The sequence of programming MTP(Internal power)

Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

8.2.28 RA2H (PGM_CFG): MTP Program Config Register

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM_CFG	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	W	1	-	-	-	VMTPSEL	-	-	M_dis	S_dis	00h
2nd Parameter	W	1	PGM_SADDR[15:8]								00h
3rd Parameter	W	1	PGM_SADDR[7:0]								00h
4th Parameter	W	1	PGM_DSIZE[15:8]								0Fh
5th Parameter	W	1	PGM_DSIZE[7:0]								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is used for setting configuration of MTP

1st Parameter:

Bit	Name	Description
0	S_dis	0: slave enable some command (default) 1: slave disable some command
1	M_dis	0: master enable some command (default) 1: master disable some command
4	VMTPSEL	0:External VMTP (default) 1:Internal VMTP

Bit[0] enable/disable some command when IC sets slave (MS pin is low)
Bit[1] enable/disable some command when IC sets master (MS pin is high)

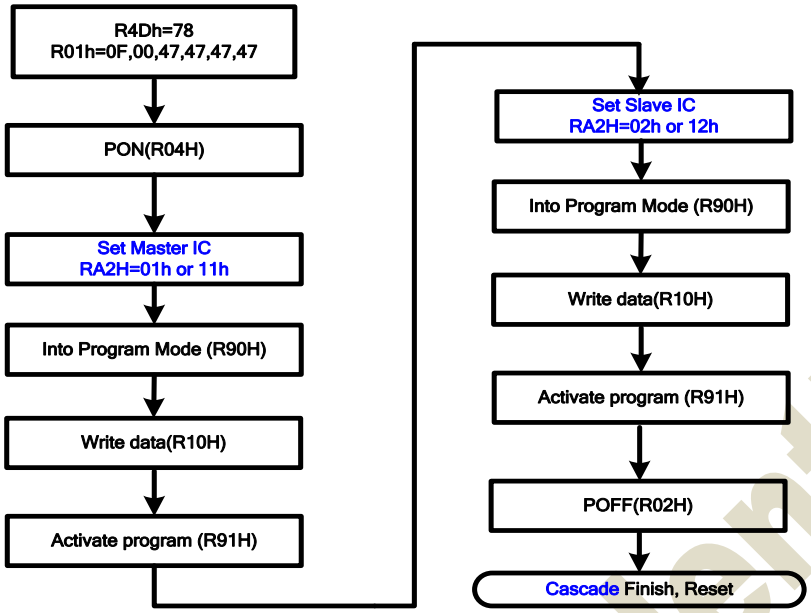
Note:
Some command define: R00H(Parameter 1) (PSR), R10H(DTM), R90H(PGM), R91H(APG), R83H(PTLW)

Command read

M_dis	S_dis	Description
0	0	command read from master
0	1	command read from master
1	0	command read from slave
1	1	command read from slave

2nd & 3rd Parameters: Program and Read MTP start address PGM_SADDR[15:0]
4th & 5th Parameters: Program data size PGM_DSIZE[15:0]

Note:
If user program Area0 (0x00~0x017F), PGM_SADDR[15:0] will be set 0x0000, PGM_DSIZE[15:0] will be set 0x0180.

	Cascade MTP Flow 
Restriction	

8.2.29 RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	-	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade. 1st Parameter:

Bit	Name	Description
0	CCEIN	Output clock enable/disable. 0: Output 0V at SyncC pin. (default) 1: Output clock at SyncC pin for slave chip.

Restriction	

8.2.30 RE3H (PWS): Power Saving Register

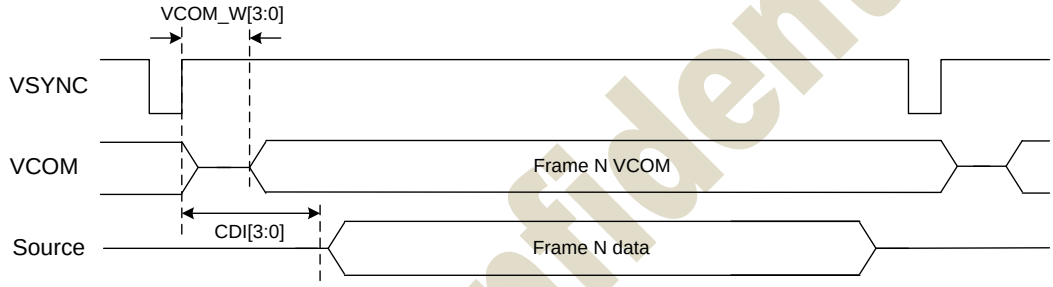
RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h
2st Parameter	W	1	-	GD_WR[2:0]			-	GD_WF[2:0]			00h

NOTE: "-" Don't care, can be set to VDD or GND level

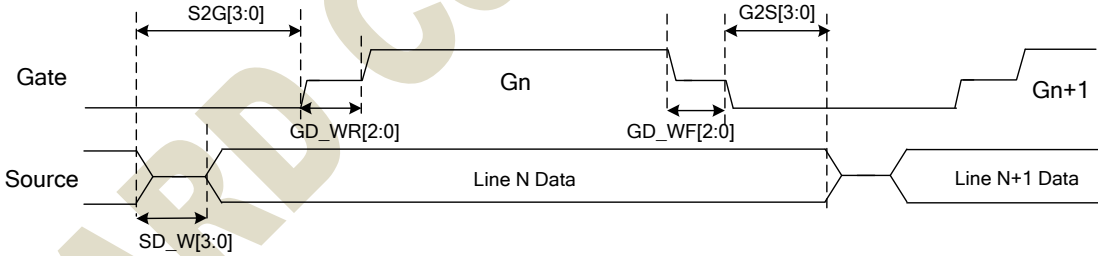
Description

- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W: VCOM power saving width (unit = line period)



SD_W: Source power saving width (unit = 500nS), SD_W<=S2G
GD_WR/GD_WF: Gate power saving width (unit = 500nS)



Gon_T = 1 line period – S2G – G2S – GD_WR – GD_WF, Gon_T min= 2 units.

Restriction

8.2.31 RE4H (LVSEL): LVD Voltage Select Register

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	LVD_SEL[1:0]: Low Power Voltage Selection
Restriction	

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

Register Restriction

Following table will indicate the register restriction:

Register	Refresh Restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R04H(PON)	X	Flag
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM1)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R17H(AUTO)	Valid in standby	Flag
R30H(PLL)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R61H(TRES)	X	No action
R65H(GSST)	X	No action
R70H(REV)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
R83H(PTL)	X	No action
R90H(PGM)	X	No action
R91H(APG)	X	Flag
R92H(RMTP)	X	Flag
RA2H(PGM_CFG)	X	No action
RE0H(CCSET)	X	No action
RE3H(PWS)	X	No action
RE4H(LVSEL)	X	No action

9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power on Sequence

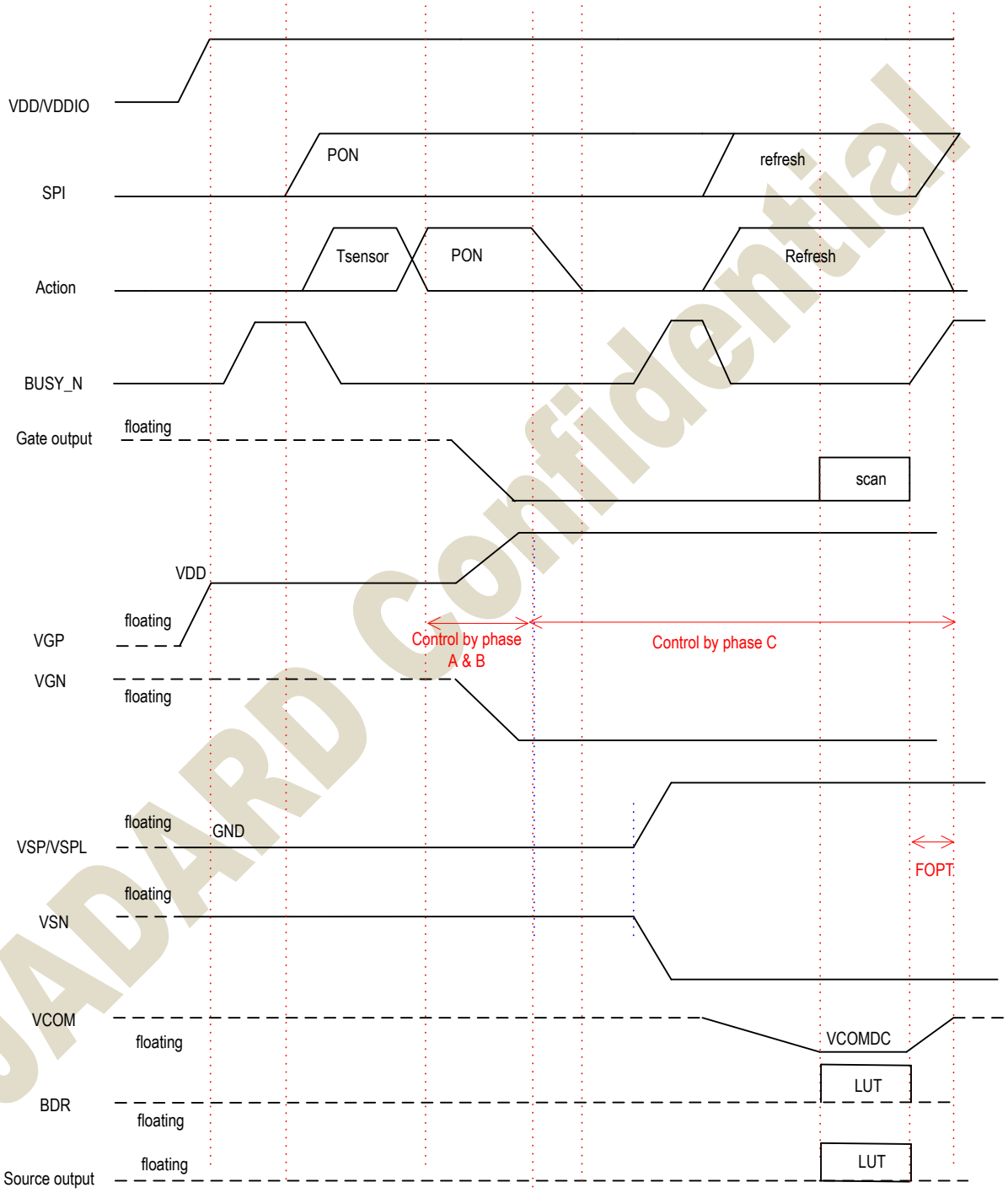


Figure 1: Power on sequence (TPS=LOW)

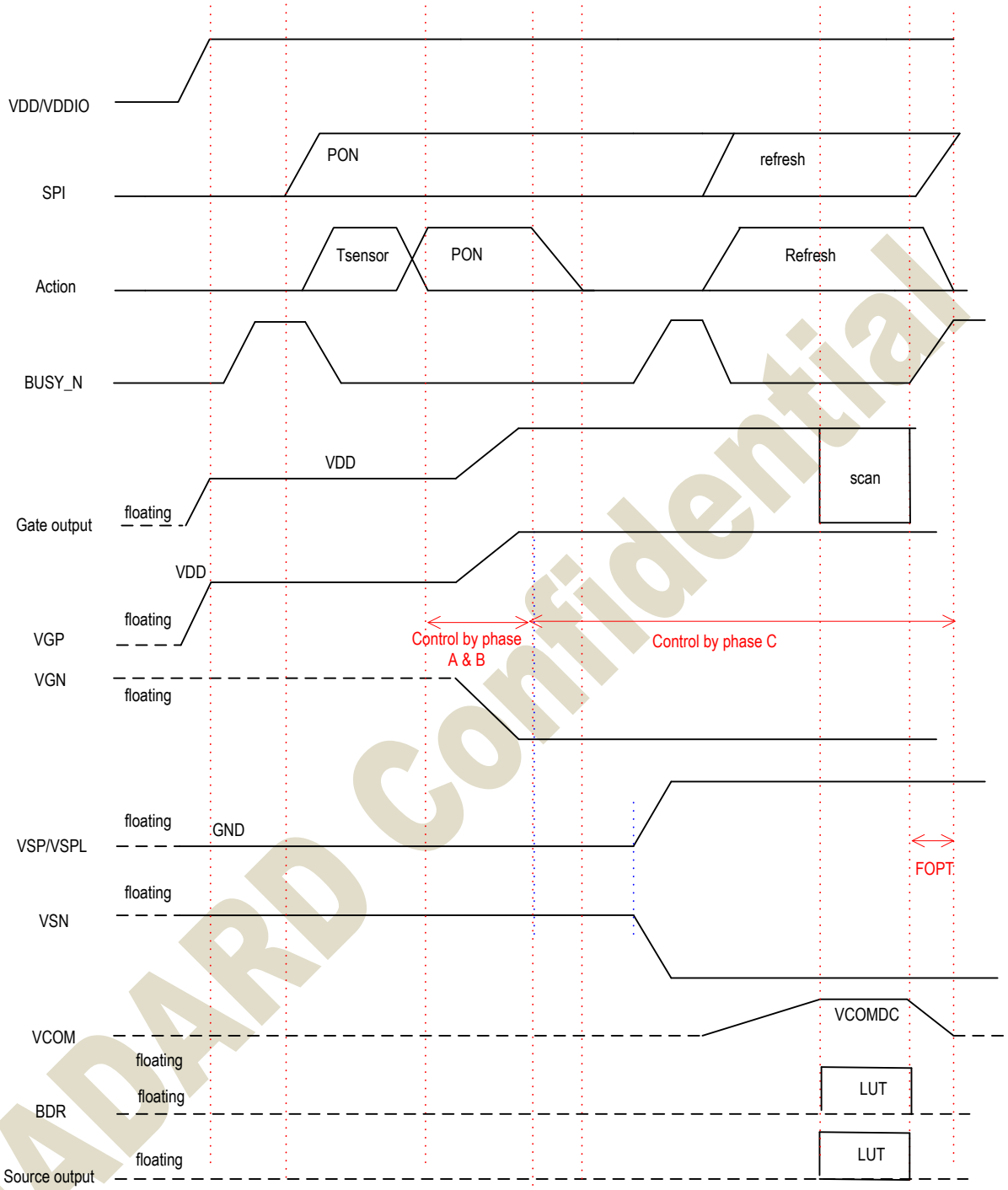


Figure 2: Power on sequence (TPS=HIGH)

Power off Sequence

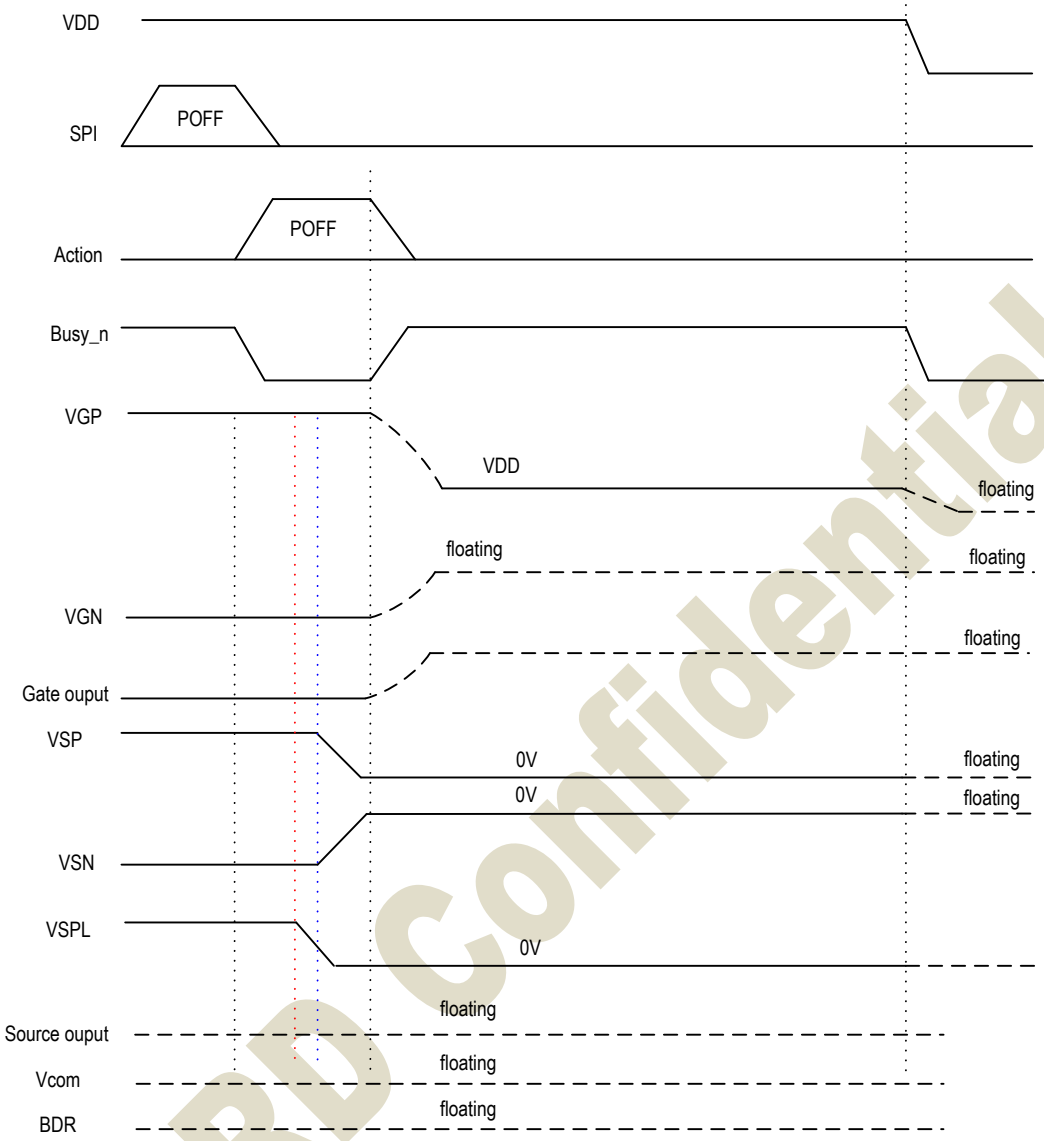


Figure 3: Power off sequence (TPS=LOW)

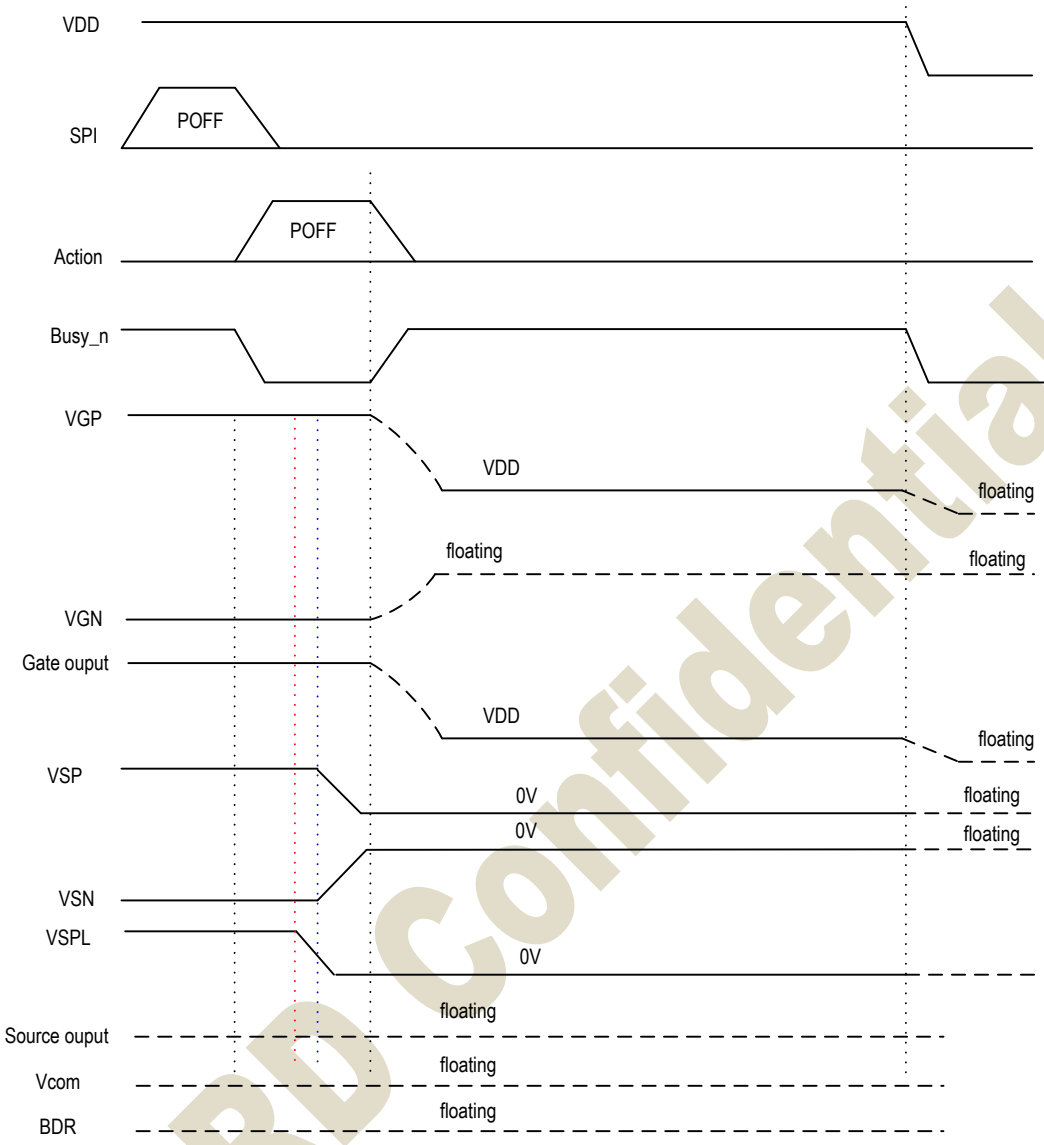


Figure 4: Power off sequence (TPS=HIGH)

DSLP sequence

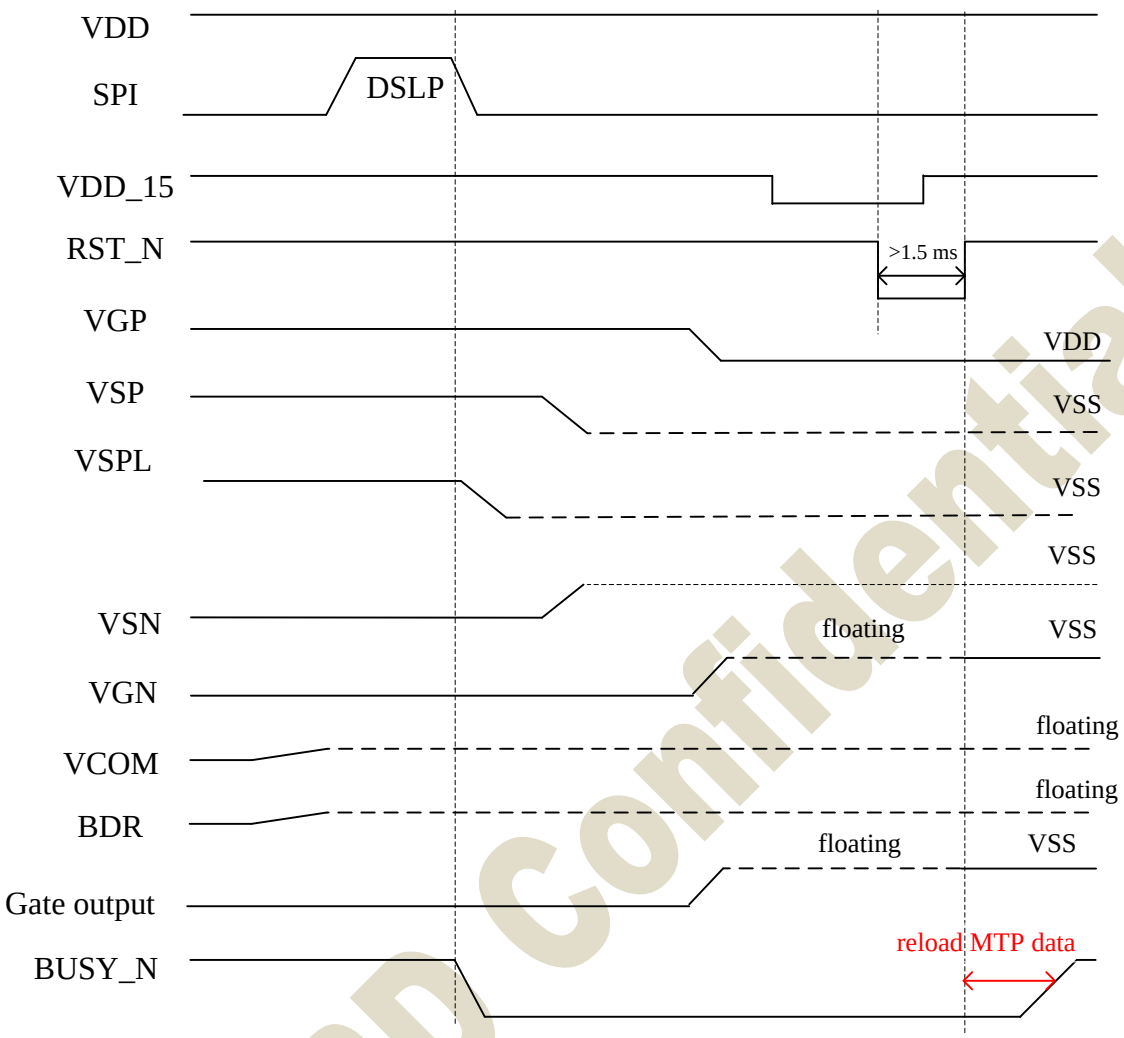


Figure 5: DSLP sequence (TPS=LOW)

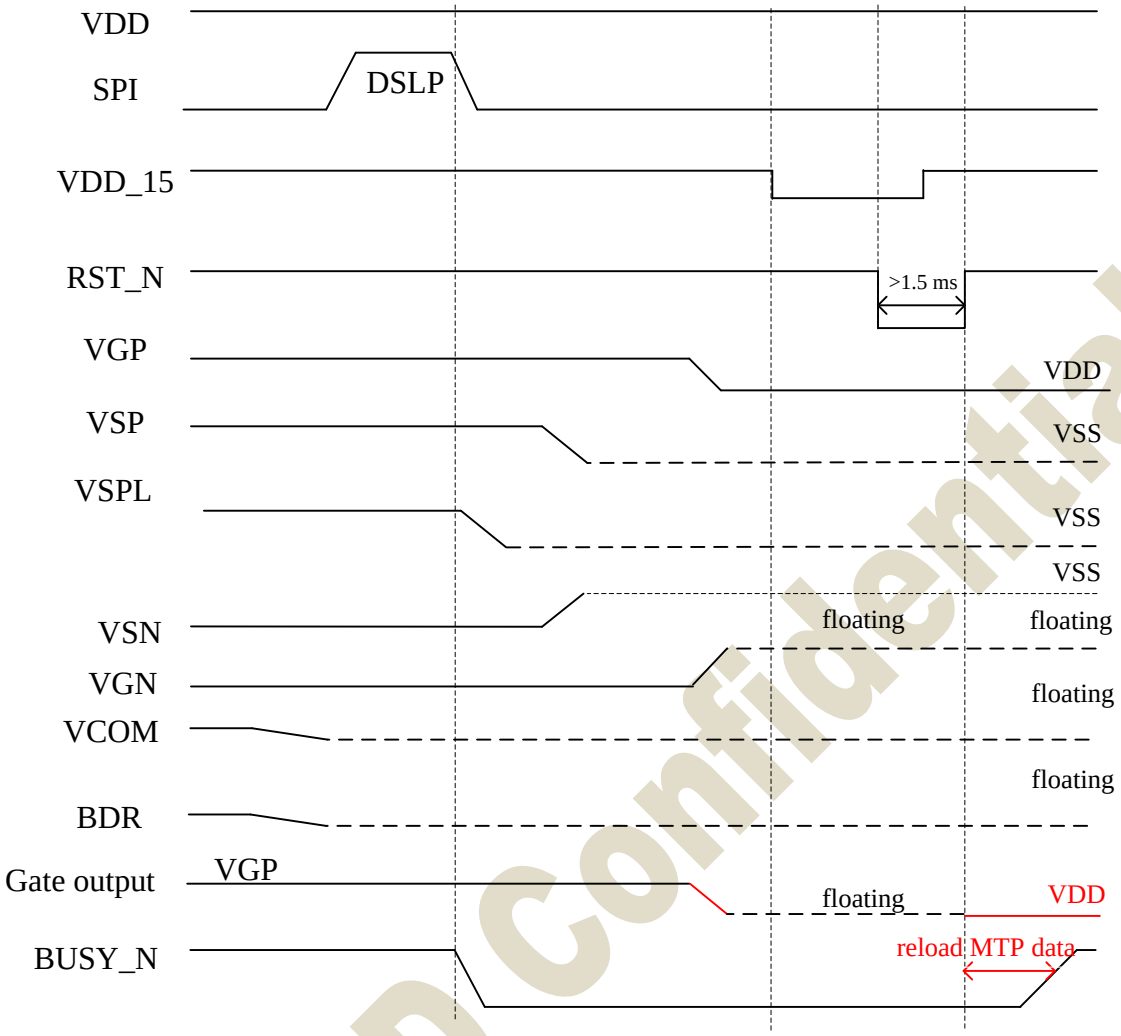


Figure 6: DSLP sequence (TPS=HIGH)

9.2 MTP LUT Definition

The MTP size would be 4096 Bytes.

MTP bank 0 (4K bytes)	
Address(Hex)	Content
0x000~0xEFF	LUT Compress data
0xF00~0xF58	Reserved
0xF59~0xF84	Default setting
0xF85~0xFFF	JD setting

9.3 Default Setting Format in MTP

	Addr. (Dec)	Addr. (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value (Hex)
	-	-	User Reserved bytes								00
--	3927	F57	Enable MTP Setting (0xA5)								A5
RE3h	3928	F58	VCOM_W[3:0]				SD_W[3:0]				00
	3929	F59	-	GD_WR[2:0]			-	GD_WF[2:0]			00
-	3930	F5A	Reserved								-
	3931	F5B	Reserved								-
R00H	3932	F5C	RES[1:0]		PST_MODE	-	UD	SHL	SHD_N	RST_N	0F
	3933	F5D	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09
R01H	3934	F5E	-	-	BD_EN	-	-	VSC_EN	VDS_EN	VDG_EN	07
	3935	F5F	-	-	-	-	-	-	VGP[1:0]		00
	3936	F60	-	VSPL_0[6:0]							00
	3937	F61	-	VSP_1[6:0]							00
	3938	F62	-	VSN_1[6:0]							00
	3939	F63	-	VSPL_1[6:0]							00
-	3940	F64	Reserved								00
	3941	F65	Reserved								00
	3942	F66	Reserved								54
	3943	F67	Reserved								44
R06H	3944	F68	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00
	3945	F69	-	-	PHA_ON[5:0]						06
	3946	F6A	-	-	PHA_OFF[5:0]						02
	3947	F6B	-	-	PHB_ON[5:0]						07
	3948	F6C	-	-	PHB_OFF[5:0]						02
	3949	F6D	-	-	PHC_ON[5:0]						07
	3950	F6E	-	-	PHC_OFF[5:0]						02
-	3951	F6F	Reserved								00
R30H	3952	F70	-	-	-	-	Dyna	FR[2:0]			02
R50h	3953	F71	VBD[2:0]			DDX	CDI[3:0]				97
-	3954	F72	Reserved								02
	3955	F73	Reserved								02
R61H	3956	F74	-	-	-	-	-	-	HRES[9]	HRES[8]	00
	3957	F75	HRES[7:2]						0	0	00
	3958	F76	-	-	-	-	-	-	VRES[9]	VRES[8]	00
	3959	F77	VRES[7:0]								00
R65H	3960	F78	-	-	-	-	-	-	S_start(9)	S_start(8)	00
	3961	F79	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00
	3962	F7A	-	-	-	-	-	-	G_start(9)	G_start(8)	00
	3963	F7B	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00
R82H	3964	F7C		VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00
-	3965	F7D	Reserved								00
R41H	3966	F7E	-	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00
-	3967	F7F	Reserved								00
	3968	F80	Reserved								00
RE4H	3969	F81	-	-	-	-	-		LVD_SEL[1:0]		03
-	3970	F82	Reserved								03
	3971	F83	Reserved								1C
	3972	F84	Reserved								00
-	3973-4095	F85-FFF	JD setting								FF

9.4 Data transmission waveform

Example1: The driver will scan 1 frame to GND after waveform finished.(FOPT=0)

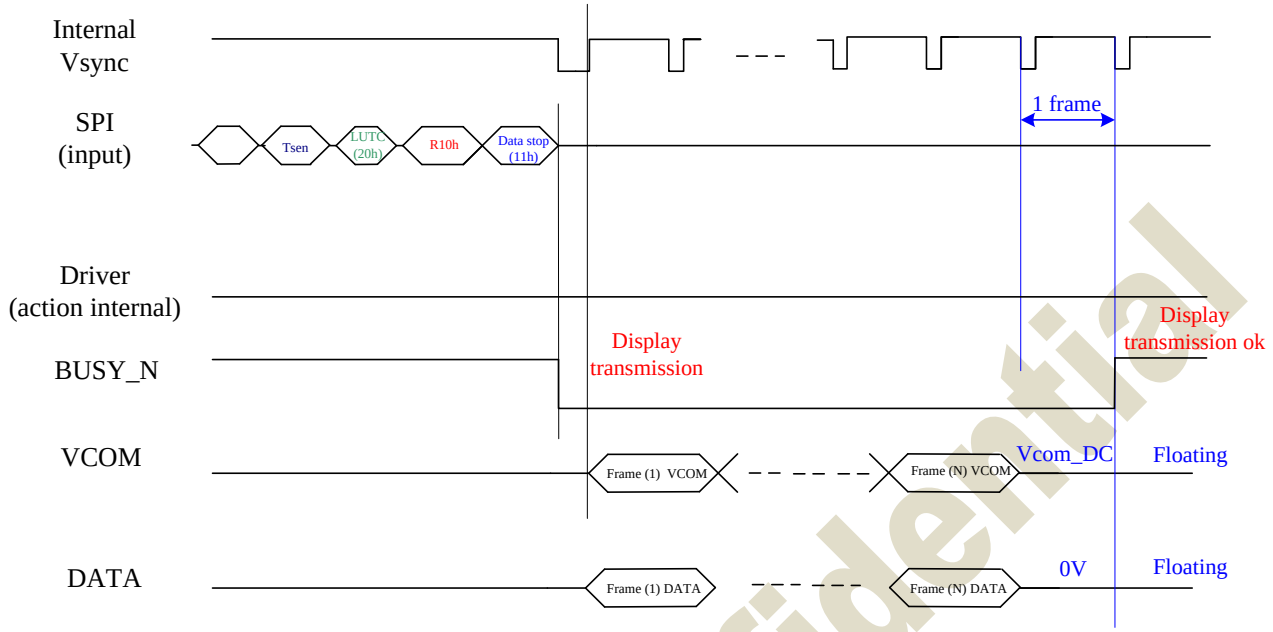


Figure 1: Data transmission example1 waveform

Example2: The driver will float VCOM and keep previous output data(FOPT=1)

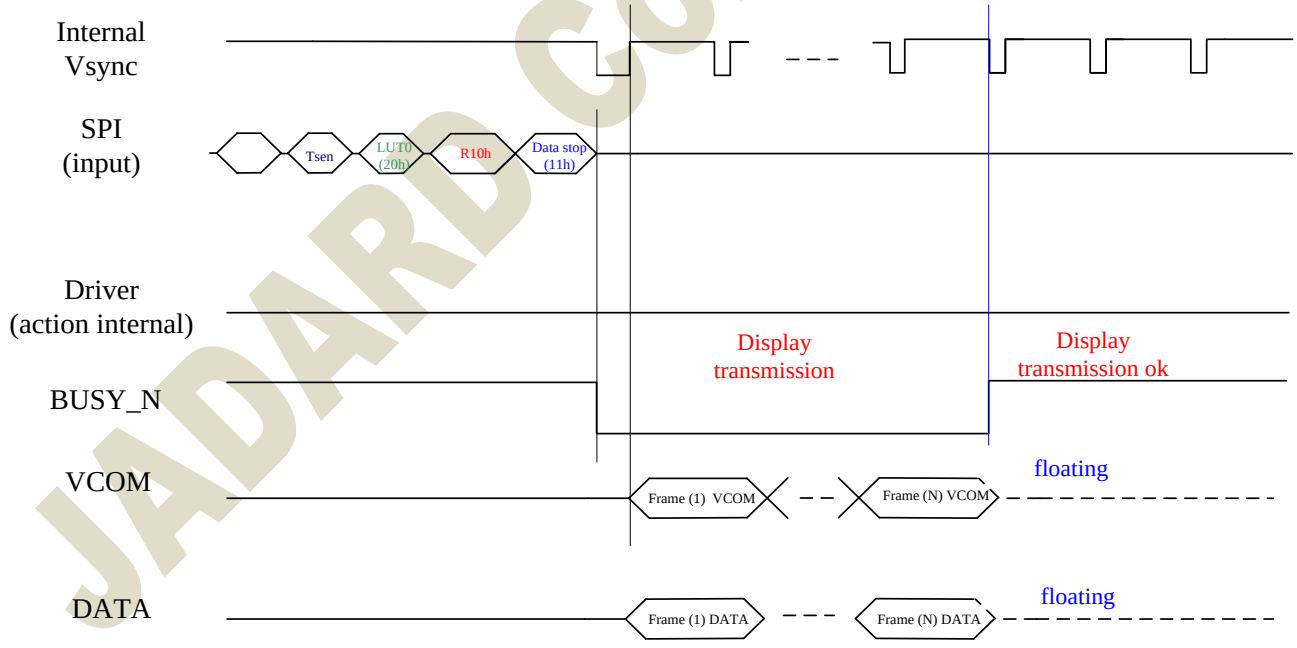


Figure 2: Display refresh example2 waveform

10. ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	VDDIO+0.3	V
Supply range	VGP-VGN	VGN-0.3	VGP+0.3	V
Analog supply	VSP_0	+15	+15	V
Analog supply	VSN_0	-15	-15	V
Analog supply	VSPL_0	+3	+15	V
Analog supply	VSP_1	+3	+15	V
Analog supply	VSN_1	-3	-15	V
Analog supply	VSPL_1	+3	+15	V
Supply voltage	VGP	+10	+20	V
Supply voltage	VGN	-20	-10	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

10.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.5V output voltage	VDD_15	1.35	1.5	1.65		
1.5V input voltage	VDD_15	1.35	1.5	1.65		
MTP program power	VMTP	9.8	10.1	10.2		
Digital ground	VSS		0			
DCDC ground	VSSP		0			
Low Level Input Voltage	Vil	GND	-	0.3Xvdd	V	Digital input pins
High Level Input Voltage	Vih	0.7Xvio	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400Ma
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400Ma DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL = -400Ma
Input Leakage Current	Iin	-1.0	-	+1.0	Ua	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Digital Stand-by Current (power off mode)	IstVDD*	-	0	1	Ua	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	Ma	
IO Stand-by Current (power off mode)	IstVDDIO*	-	0.4	1.0	Ua	All stopped
IO Operating Current	IVDDIO*	-	-	0.2	Ma	No load
Operating Current	IVDD1*	-	-	TBD	Ma	
Operating temperature	T_{op}	-30	-	85	℃	

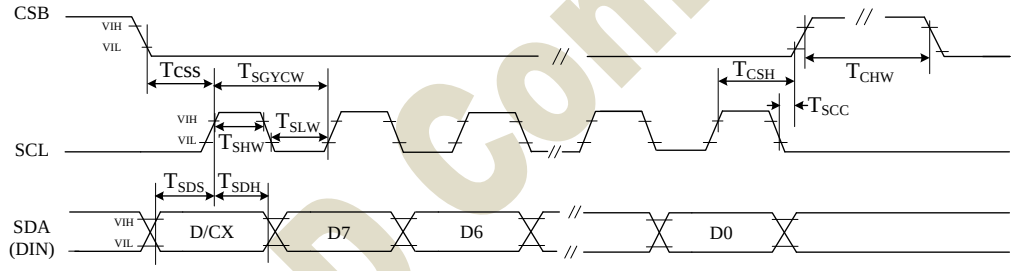
NOTE: typ. And max. values to be confirmed by design

10.3 Analog DC Characteristics

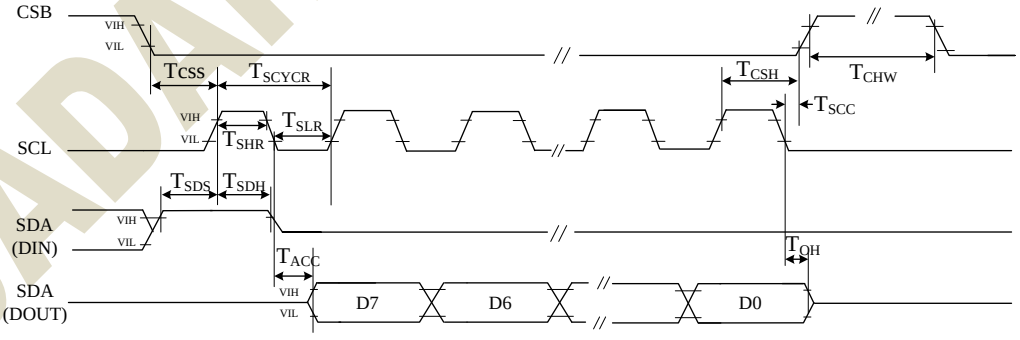
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSP	-	15	-	V	For source driver/VCOM
Positive Source voltage dev	Dvsp	-100	0	+100	Mv	
Negative Source voltage	VSn	-	-15	-	V	For source driver/VCOM
Negative Source voltage dev	Dvsn	-100	-	+100	Mv	
Positive Source voltage	VSPL_0	3		15		
Positive Source voltage dev.	Dvspl_0	-100	-	+100	Mv	
Positive Source voltage	VSP_1	3		15		
Positive Source voltage dev.	Dvsp_1	-100	-	+100	Mv	
Positive Source voltage	VSPL_1	3		15		
Positive Source voltage dev.	Dvspl_1	-100	-	+100	Mv	
VCOM voltage dev.	Dvcom	-200	-	+200	Mv	
Positive gate voltage dev	Dvgp	-500	-	+500	Mv	
Dynamic Range of Output	Vdr	0.1	-	VSP-0.1	V	
Voltage Range of VGP – VGN	VGP-VGN	-	-	41	V	
Negative Gate voltage	VGN	-10	-	-20	V	For gate driver
Positive Gate voltage	VGP	10		20	V	For gate driver
Positive HV Stand-by Current (power off mode)	IstVGP*	-	0	0.2	Ua	Include VSP power With load
Positive HV Operating Current	IVGP*	-	0.7	1.1	Ma	Include VSP power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVGP*	-	0.8	1.2	Ma	Include VSP power With load all SD=H VCOM external resistor divider not Included
Negative HV Stand-by Current (power off mode)	IstVGN*	-	0	0.2	Ma	Include VSP power With load
Negative HV Operating Current	IVGN*	-	0.8	1.2	Ma	Include VSN power With load all SD=L
Negative HV Operating Current	IVGN*	-	0.9-	1.3	Ma	Include VSN power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*	-	0	0.01	Ma	
VINT1 Operating Current	IVINT1*	-	-	0.3	Ma	
Voltage	IVINT1*	-	-	0.3	Ma	

10.4 AC Characteristics

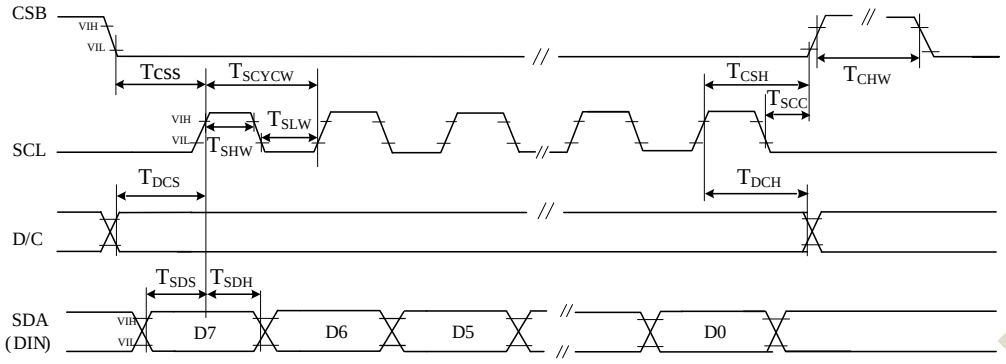
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	60			ns	Chip select setup time
	T_{CSH}	65			ns	Chip select hold time
	T_{SCC}	20			ns	Chip select CSB setup time
	T_{CHW}	40			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35			ns	SCL “H” pulse width (Write)
	T_{SLW}	35			ns	SCL “L” pulse width (Write)
	T_{SCYCR}	250			ns	Serial clock cycle (Read)
	T_{SHR}	60			ns	SCL “H” pulse width (Read)
	T_{SLR}	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}			50	ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time



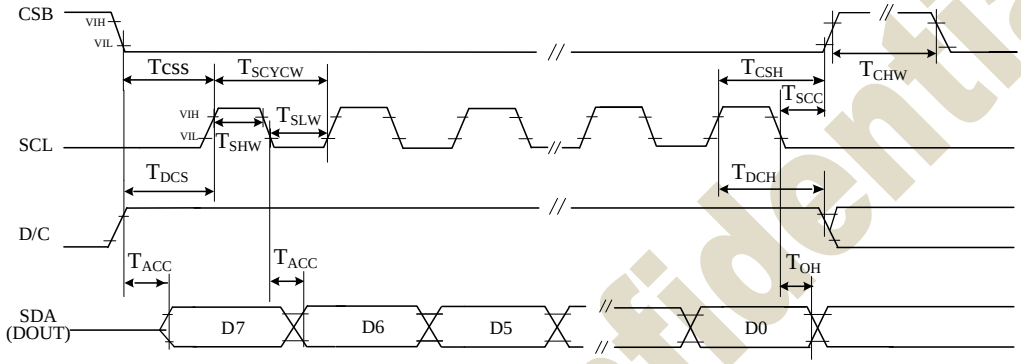
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)

Figure 9: SPI interface timing

11. CHIP OUTLINE DIMENSIONS

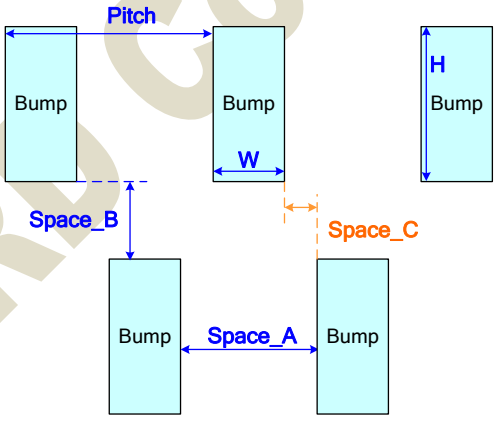
11.1 Circuit/Bump View

G1 G3 G5 ... S799 ~ S0 ... G4 G2 G0

JD79665
(face up)

Die Size: 18490um*1106um
Die Size :18550um*1166um (Including Scribe Line 60um)
Die Thickness: 230 μm ± 20μm
Die TTV:(DMAX – DMIN) within die ≤ 2μm
Bump Height: 9 μm ± 2μm
(HMAX – HMIN) within die ≤ 2μm
Hardness: 75 Hv ±25Hv
Coordinate origin:Chip center

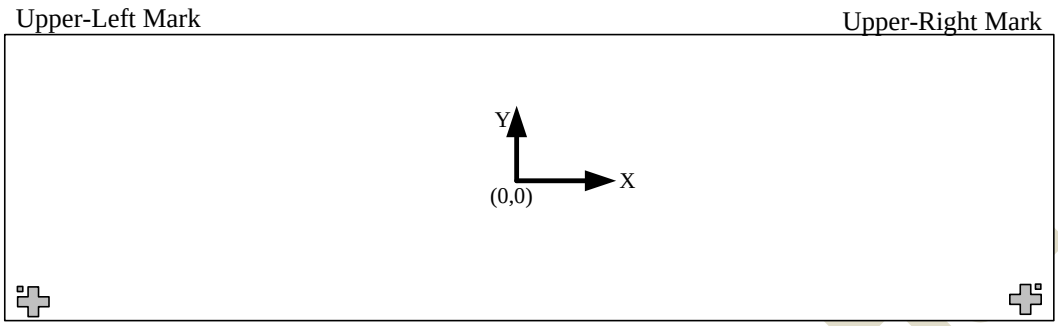
11.2 Bump information



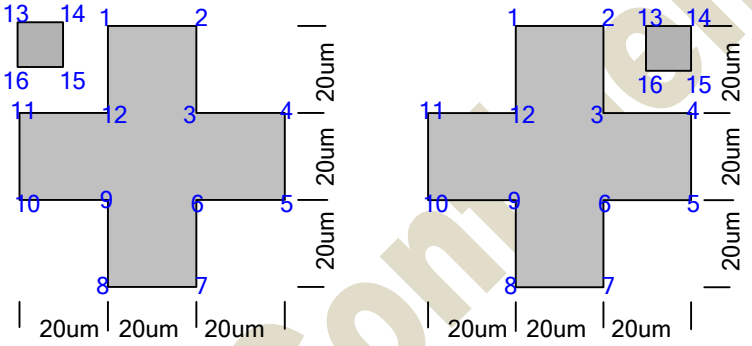
Bump type	Pitch	Space_A	Space_B	Space_C	W	H	area(um2)	Q'ty	Total Area(um2)
Input PAD	46	14	-	-	32	70	2240	395	884800
Source PAD	26	14	29	0.1	12	84	1008	806	812448
Gate PAD	25	12	-	-	12	84	1008	616	620928
							Total	1817	2318176

12. ALIGNMENT MARK INFORMATION

12.1 Location



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-9183.0	-496.0	9183.0	-496.0
1	-9193.0	-466.0	9173.0	-466.0
2	-9173.0	-466.0	9193.0	-466.0
3	-9173.0	-486.0	9193.0	-486.0
4	-9153.0	-486.0	9213.0	-486.0
5	-9153.0	-506.0	9213.0	-506.0
6	-9173.0	-506.0	9193.0	-506.0
7	-9173.0	-526.0	9193.0	-526.0
8	-9193.0	-526.0	9173.0	-526.0
9	-9193.0	-506.0	9173.0	-506.0
10	-9213.0	-506.0	9153.0	-506.0
11	-9213.0	-486.0	9153.0	-486.0
12	-9193.0	-486.0	9173.0	-486.0
13	-9213.0	-466.0	9203.0	-466.0
14	-9203.0	-466.0	9213.0	-466.0
15	-9203.0	-476.0	9213.0	-476.0
16	-9213.0	-476.0	9203.0	-476.0

12.2 Pad coordinates

No.	Name	X-axis	Y-axis	W	H
1	DUMMY[0]	-9062	-508	32	70
2	DUMMY[1]	-9016	-508	32	70
3	VCOM	-8970	-508	32	70
4	VCOM	-8924	-508	32	70
5	VCOM	-8878	-508	32	70
6	VCOM	-8832	-508	32	70
7	VCOM	-8786	-508	32	70
8	VCOM	-8740	-508	32	70
9	VCOM	-8694	-508	32	70
10	VCOM	-8648	-508	32	70
11	VCOM	-8602	-508	32	70
12	VCOM	-8556	-508	32	70
13	VCOM	-8510	-508	32	70
14	VCOM	-8464	-508	32	70
15	VCOM	-8418	-508	32	70
16	VCOM	-8372	-508	32	70
17	VCOM	-8326	-508	32	70
18	VCOM	-8280	-508	32	70
19	VCOM	-8234	-508	32	70
20	VCOM	-8188	-508	32	70
21	VCOM	-8142	-508	32	70
22	VSSA	-8096	-508	32	70
23	VGN	-8050	-508	32	70
24	VGN	-8004	-508	32	70
25	VGN	-7958	-508	32	70
26	VGN	-7912	-508	32	70
27	VGN	-7866	-508	32	70
28	VGN	-7820	-508	32	70
29	VGN	-7774	-508	32	70
30	VGN	-7728	-508	32	70
31	VGN	-7682	-508	32	70
32	VGN	-7636	-508	32	70
33	VGN	-7590	-508	32	70
34	VGN	-7544	-508	32	70
35	VGN	-7498	-508	32	70
36	VGN	-7452	-508	32	70
37	VSSA	-7406	-508	32	70
38	VSN	-7360	-508	32	70
39	VSN	-7314	-508	32	70
40	VSN	-7268	-508	32	70
41	VSN	-7222	-508	32	70
42	VSN	-7176	-508	32	70
43	VSN	-7130	-508	32	70
44	VSN	-7084	-508	32	70
45	VSN	-7038	-508	32	70
46	VSN	-6992	-508	32	70
47	VSN	-6946	-508	32	70
48	VSN	-6900	-508	32	70
49	VSN	-6854	-508	32	70
50	VSSA	-6808	-508	32	70
51	VGP	-6762	-508	32	70
52	VGP	-6716	-508	32	70
53	VGP	-6670	-508	32	70
54	VGP	-6624	-508	32	70
55	VGP	-6578	-508	32	70
56	VGP	-6532	-508	32	70
57	VGP	-6486	-508	32	70
58	VGP	-6440	-508	32	70
59	VGP	-6394	-508	32	70
60	VGP	-6348	-508	32	70

No.	Name	X-axis	Y-axis	W	H
61	VGP	-6302	-508	32	70
62	VGP	-6256	-508	32	70
63	VGP	-6210	-508	32	70
64	VGP	-6164	-508	32	70
65	VSSA	-6118	-508	32	70
66	VSP	-6072	-508	32	70
67	VSP	-6026	-508	32	70
68	VSP	-5980	-508	32	70
69	VSP	-5934	-508	32	70
70	VSP	-5888	-508	32	70
71	VSP	-5842	-508	32	70
72	VSP	-5796	-508	32	70
73	VSP	-5750	-508	32	70
74	VSP	-5704	-508	32	70
75	VSP	-5658	-508	32	70
76	VSP	-5612	-508	32	70
77	VSP	-5566	-508	32	70
78	VSSA	-5520	-508	32	70
79	VMTP	-5474	-508	32	70
80	VMTP	-5428	-508	32	70
81	VMTP	-5382	-508	32	70
82	VMTP	-5336	-508	32	70
83	VMTP	-5290	-508	32	70
84	VMTP	-5244	-508	32	70
85	VMTP	-5198	-508	32	70
86	VMTP	-5152	-508	32	70
87	VMTP	-5106	-508	32	70
88	VMTP	-5060	-508	32	70
89	DUMMY[2]	-5014	-508	32	70
90	T_N18V	-4968	-508	32	70
91	T_LDON5V	-4922	-508	32	70
92	DUMMY[3]	-4876	-508	32	70
93	DUMMY[4]	-4830	-508	32	70
94	DUMMY[5]	-4784	-508	32	70
95	DUMMY[6]	-4738	-508	32	70
96	DUMMY[7]	-4692	-508	32	70
97	DUMMY[8]	-4646	-508	32	70
98	DUMMY[9]	-4600	-508	32	70
99	DUMMY[10]	-4554	-508	32	70
100	DUMMY[11]	-4508	-508	32	70
101	DUMMY[12]	-4462	-508	32	70
102	DUMMY[13]	-4416	-508	32	70
103	VDD_15V	-4370	-508	32	70
104	VDD_15V	-4324	-508	32	70
105	VDD_15V	-4278	-508	32	70
106	VDD_15V	-4232	-508	32	70
107	VDD_15V	-4186	-508	32	70
108	VDD_15V	-4140	-508	32	70
109	VDD_15V	-4094	-508	32	70
110	VDD_15V	-4048	-508	32	70
111	VDD_15V	-4002	-508	32	70
112	VDD_15V	-3956	-508	32	70
113	VDD_15V	-3910	-508	32	70
114	VDD_15V	-3864	-508	32	70
115	VDD_15V	-3818	-508	32	70
116	VDD_15V	-3772	-508	32	70
117	VDD_15V	-3726	-508	32	70
118	VDD_15V	-3680	-508	32	70
119	VSSA	-3634	-508	32	70
120	VSSA	-3588	-508	32	70

No.	Name	X-axis	Y-axis	W	H
121	VSSA	-3542	-508	32	70
122	VSSA	-3496	-508	32	70
123	VSSA	-3450	-508	32	70
124	VSSA	-3404	-508	32	70
125	VSSA	-3358	-508	32	70
126	VSSA	-3312	-508	32	70
127	VSSA	-3266	-508	32	70
128	VSSA	-3220	-508	32	70
129	VSSA	-3174	-508	32	70
130	VSSA	-3128	-508	32	70
131	VSS	-3082	-508	32	70
132	VSS	-3036	-508	32	70
133	VSS	-2990	-508	32	70
134	VSS	-2944	-508	32	70
135	VSS	-2898	-508	32	70
136	VSS	-2852	-508	32	70
137	VSS	-2806	-508	32	70
138	VSS	-2760	-508	32	70
139	VSS	-2714	-508	32	70
140	VSS	-2668	-508	32	70
141	VSS	-2622	-508	32	70
142	VSS	-2576	-508	32	70
143	VDD	-2530	-508	32	70
144	VDD	-2484	-508	32	70
145	VDD	-2438	-508	32	70
146	VDD	-2392	-508	32	70
147	VDD	-2346	-508	32	70
148	VDD	-2300	-508	32	70
149	VDD	-2254	-508	32	70
150	VDD	-2208	-508	32	70
151	VDD	-2162	-508	32	70
152	VDD	-2116	-508	32	70
153	VDDIO	-2070	-508	32	70
154	VDDIO	-2024	-508	32	70
155	VDDIO	-1978	-508	32	70
156	VDDIO	-1932	-508	32	70
157	VDDIO	-1886	-508	32	70
158	VDDIO	-1840	-508	32	70
159	VDDIO	-1794	-508	32	70
160	VDDIO	-1748	-508	32	70
161	VDDIO	-1702	-508	32	70
162	VDDIO	-1656	-508	32	70
163	VDDIO	-1610	-508	32	70
164	DUMMY[14]	-1564	-508	32	70
165	DUMMY[15]	-1518	-508	32	70
166	DUMMY[16]	-1472	-508	32	70
167	DUMMY[17]	-1426	-508	32	70
168	DUMMY[18]	-1380	-508	32	70
169	DUMMY[19]	-1334	-508	32	70
170	DUMMY[20]	-1288	-508	32	70
171	T_VCOM	-1242	-508	32	70
172	T_EN_LSH	-1196	-508	32	70
173	T_IBIAS	-1150	-508	32	70
174	T_VREF	-1104	-508	32	70
175	T_VTSEN	-1058	-508	32	70
176	T_SAR_REF	-1012	-508	32	70
177	T_VSPD_REF	-966	-508	32	70
178	DUMMY[21]	-920	-508	32	70
179	DUMMY[22]	-874	-508	32	70
180	DUMMY[23]	-828	-508	32	70

No.	Name	X-axis	Y-axis	W	H
181	DUMMY[24]	-782	-508	32	70
182	DUMMY[25]	-736	-508	32	70
183	DUMMY[26]	-690	-508	32	70
184	DUMMY[27]	-644	-508	32	70
185	DUMMY[28]	-598	-508	32	70
186	DUMMY[29]	-552	-508	32	70
187	DUMMY[30]	-506	-508	32	70
188	DUMMY[31]	-460	-508	32	70
189	T_IN[2]	-414	-508	32	70
190	T_IN[2]	-368	-508	32	70
191	T_IN[1]	-322	-508	32	70
192	T_IN[1]	-276	-508	32	70
193	T_IN[0]	-230	-508	32	70
194	T_IN[0]	-184	-508	32	70
195	DUMMY[32]	-138	-508	32	70
196	DUMMY[33]	-92	-508	32	70
197	DUMMY[34]	-46	-508	32	70
198	DUMMY[35]	0	-508	32	70
199	DUMMY[36]	46	-508	32	70
200	DUMMY[37]	92	-508	32	70
201	DUMMY[38]	138	-508	32	70
202	DUMMY[39]	184	-508	32	70
203	T_EX_SYSCLK	230	-508	32	70
204	T_EX_SYSCLK	276	-508	32	70
205	T_EX_REFCLK	322	-508	32	70
206	T_EX_REFCLK	368	-508	32	70
207	T_EN_DIG	414	-508	32	70
208	T_EN_DIG	460	-508	32	70
209	DUMMY[40]	506	-508	32	70
210	DUMMY[41]	552	-508	32	70
211	VDDP	598	-508	32	70
212	VDDP	644	-508	32	70
213	VDDP	690	-508	32	70
214	VDDP	736	-508	32	70
215	VDDP	782	-508	32	70
216	VDDP	828	-508	32	70
217	VDDP	874	-508	32	70
218	VDDP	920	-508	32	70
219	VDDP	966	-508	32	70
220	VDDP	1012	-508	32	70
221	VDDP	1058	-508	32	70
222	VDDP	1104	-508	32	70
223	VDDP	1150	-508	32	70
224	DUMMY[42]	1196	-508	32	70
225	DUMMY[43]	1242	-508	32	70
226	SDA	1288	-508	32	70
227	SDA	1334	-508	32	70
228	SCL	1380	-508	32	70
229	SCL	1426	-508	32	70
230	VSS	1472	-508	32	70
231	CSB	1518	-508	32	70
232	CSB	1564	-508	32	70
233	VDDIO	1610	-508	32	70
234	DUMMY[44]	1656	-508	32	70
235	DUMMY[45]	1702	-508	32	70
236	VSS	1748	-508	32	70
237	DC	1794	-508	32	70
238	DC	1840	-508	32	70
239	VDDIO	1886	-508	32	70
240	DUMMY[46]	1932	-508	32	70

No.	Name	X-axis	Y-axis	W	H
241	DUMMY[47]	1978	-508	32	70
242	RST_N	2024	-508	32	70
243	RST_N	2070	-508	32	70
244	BUSY_N	2116	-508	32	70
245	BUSY_N	2162	-508	32	70
246	VSS	2208	-508	32	70
247	DUMMY[48]	2254	-508	32	70
248	SYNCE	2300	-508	32	70
249	SYNCD	2346	-508	32	70
250	SYNCC	2392	-508	32	70
251	SYNCC	2438	-508	32	70
252	SYNCD	2484	-508	32	70
253	SYNCD	2530	-508	32	70
254	SYNCE	2576	-508	32	70
255	SYNCE	2622	-508	32	70
256	DUMMY[49]	2668	-508	32	70
257	DUMMY[50]	2714	-508	32	70
258	DUMMY[51]	2760	-508	32	70
259	DUMMY[52]	2806	-508	32	70
260	VSS	2852	-508	32	70
261	DUMMY[53]	2898	-508	32	70
262	DUMMY[54]	2944	-508	32	70
263	VDDIO	2990	-508	32	70
264	DUMMY[55]	3036	-508	32	70
265	DUMMY[56]	3082	-508	32	70
266	TPS	3128	-508	32	70
267	DUMMY[57]	3174	-508	32	70
268	VDDIO	3220	-508	32	70
269	BS	3266	-508	32	70
270	BS	3312	-508	32	70
271	VSS	3358	-508	32	70
272	DUMMY[58]	3404	-508	32	70
273	VDDIO	3450	-508	32	70
274	PCKI	3496	-508	32	70
275	PCKI	3542	-508	32	70
276	VSS	3588	-508	32	70
277	MS	3634	-508	32	70
278	MS	3680	-508	32	70
279	VDDIO	3726	-508	32	70
280	VSS	3772	-508	32	70
281	TSDA	3818	-508	32	70
282	TSDA	3864	-508	32	70
283	VDDIO	3910	-508	32	70
284	TSCL	3956	-508	32	70
285	TSCL	4002	-508	32	70
286	VSS	4048	-508	32	70
287	PCKO	4094	-508	32	70
288	PCKO	4140	-508	32	70
289	DUMMY[59]	4186	-508	32	70
290	DUMMY[60]	4232	-508	32	70
291	DUMMY[61]	4278	-508	32	70
292	DUMMY[62]	4324	-508	32	70
293	DUMMY[63]	4370	-508	32	70
294	DUMMY[64]	4416	-508	32	70
295	DUMMY[65]	4462	-508	32	70
296	DUMMY[66]	4508	-508	32	70
297	DUMMY[67]	4554	-508	32	70
298	DUMMY[68]	4600	-508	32	70
299	DUMMY[69]	4646	-508	32	70
300	DUMMY[70]	4692	-508	32	70

No.	Name	X-axis	Y-axis	W	H
301	DUMMY[71]	4738	-508	32	70
302	DUMMY[72]	4784	-508	32	70
303	DUMMY[73]	4830	-508	32	70
304	DUMMY[74]	4876	-508	32	70
305	DUMMY[75]	4922	-508	32	70
306	T_DEBUG[8]	4968	-508	32	70
307	T_DEBUG[8]	5014	-508	32	70
308	T_DEBUG[7]	5060	-508	32	70
309	T_DEBUG[7]	5106	-508	32	70
310	T_DEBUG[6]	5152	-508	32	70
311	T_DEBUG[6]	5198	-508	32	70
312	T_DEBUG[5]	5244	-508	32	70
313	T_DEBUG[5]	5290	-508	32	70
314	T_DEBUG[4]	5336	-508	32	70
315	T_DEBUG[4]	5382	-508	32	70
316	T_DEBUG[3]	5428	-508	32	70
317	T_DEBUG[3]	5474	-508	32	70
318	DUMMY[76]	5520	-508	32	70
319	DUMMY[77]	5566	-508	32	70
320	DUMMY[78]	5612	-508	32	70
321	DUMMY[79]	5658	-508	32	70
322	DUMMY[80]	5704	-508	32	70
323	DUMMY[81]	5750	-508	32	70
324	DUMMY[82]	5796	-508	32	70
325	DUMMY[83]	5842	-508	32	70
326	T_DEBUG[2]	5888	-508	32	70
327	T_DEBUG[2]	5934	-508	32	70
328	T_DEBUG[1]	5980	-508	32	70
329	T_DEBUG[1]	6026	-508	32	70
330	T_DEBUG[0]	6072	-508	32	70
331	T_DEBUG[0]	6118	-508	32	70
332	DUMMY[84]	6164	-508	32	70
333	DUMMY[85]	6210	-508	32	70
334	DUMMY[86]	6256	-508	32	70
335	VSPL	6302	-508	32	70
336	VSPL	6348	-508	32	70
337	VSPL	6394	-508	32	70
338	VSPL	6440	-508	32	70
339	VSPL	6486	-508	32	70
340	VSPL	6532	-508	32	70
341	VSPL	6578	-508	32	70
342	VSPL	6624	-508	32	70
343	VSPL	6670	-508	32	70
344	VSPL	6716	-508	32	70
345	VSPL	6762	-508	32	70
346	VSPL	6808	-508	32	70
347	VSPL	6854	-508	32	70
348	VSPL	6900	-508	32	70
349	VSPL	6946	-508	32	70
350	VSPL	6992	-508	32	70
351	DUMMY[87]	7038	-508	32	70
352	DUMMY[88]	7084	-508	32	70
353	DUMMY[89]	7130	-508	32	70
354	DUMMY[90]	7176	-508	32	70
355	DUMMY[91]	7222	-508	32	70
356	DUMMY[92]	7268	-508	32	70
357	VSSA	7314	-508	32	70
358	FB	7360	-508	32	70
359	FB	7406	-508	32	70
360	VSSA	7452	-508	32	70

No.	Name	X-axis	Y-axis	W	H
361	RESE	7498	-508	32	70
362	RESE	7544	-508	32	70
363	RESE	7590	-508	32	70
364	RESE	7636	-508	32	70
365	VSSA	7682	-508	32	70
366	GDR	7728	-508	32	70
367	GDR	7774	-508	32	70
368	GDR	7820	-508	32	70
369	GDR	7866	-508	32	70
370	GDR	7912	-508	32	70
371	GDR	7958	-508	32	70
372	GDR	8004	-508	32	70
373	GDR	8050	-508	32	70
374	GDR	8096	-508	32	70
375	GDR	8142	-508	32	70
376	GDR	8188	-508	32	70
377	GDR	8234	-508	32	70
378	GDR	8280	-508	32	70
379	GDR	8326	-508	32	70
380	VSSA	8372	-508	32	70
381	VCOM	8418	-508	32	70
382	VCOM	8464	-508	32	70
383	VCOM	8510	-508	32	70
384	VCOM	8556	-508	32	70
385	VCOM	8602	-508	32	70
386	VCOM	8648	-508	32	70
387	VCOM	8694	-508	32	70
388	VCOM	8740	-508	32	70
389	VCOM	8786	-508	32	70
390	VCOM	8832	-508	32	70
391	VCOM	8878	-508	32	70
392	VCOM	8924	-508	32	70
393	VCOM	8970	-508	32	70
394	DUMMY[93]	9016	-508	32	70
395	DUMMY[94]	9062	-508	32	70
396	G[14]	9031.5	386	12	84
397	G[10]	9056.5	386	12	84
398	G[6]	9081.5	386	12	84
399	G[2]	9106.5	386	12	84
400	DUMMY[98]	9131.5	386	12	84
401	DUMMY[96]	9156.5	386	12	84
402	DUMMY[97]	9144.5	499	12	84
403	DUMMY[95]	9169.5	499	12	84
404	G[0]	9119.5	499	12	84
405	G[4]	9094.5	499	12	84
406	G[8]	9069.5	499	12	84
407	G[12]	9044.5	499	12	84
408	G[16]	9019.5	499	12	84
409	G[18]	9006.5	386	12	84
410	G[20]	8994.5	499	12	84
411	G[22]	8981.5	386	12	84
412	G[24]	8969.5	499	12	84
413	G[26]	8956.5	386	12	84
414	G[28]	8944.5	499	12	84
415	G[30]	8931.5	386	12	84
416	G[32]	8919.5	499	12	84
417	G[34]	8906.5	386	12	84
418	G[36]	8894.5	499	12	84
419	G[38]	8881.5	386	12	84
420	G[40]	8869.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
421	G[42]	8856.5	386	12	84
422	G[44]	8844.5	499	12	84
423	G[46]	8831.5	386	12	84
424	G[48]	8819.5	499	12	84
425	G[50]	8806.5	386	12	84
426	G[52]	8794.5	499	12	84
427	G[54]	8781.5	386	12	84
428	G[56]	8769.5	499	12	84
429	G[58]	8756.5	386	12	84
430	G[60]	8744.5	499	12	84
431	G[62]	8731.5	386	12	84
432	G[64]	8719.5	499	12	84
433	G[66]	8706.5	386	12	84
434	G[68]	8694.5	499	12	84
435	G[70]	8681.5	386	12	84
436	G[72]	8669.5	499	12	84
437	G[74]	8656.5	386	12	84
438	G[76]	8644.5	499	12	84
439	G[78]	8631.5	386	12	84
440	G[80]	8619.5	499	12	84
441	G[82]	8606.5	386	12	84
442	G[84]	8594.5	499	12	84
443	G[86]	8581.5	386	12	84
444	G[88]	8569.5	499	12	84
445	G[90]	8556.5	386	12	84
446	G[92]	8544.5	499	12	84
447	G[94]	8531.5	386	12	84
448	G[96]	8519.5	499	12	84
449	G[98]	8506.5	386	12	84
450	G[100]	8494.5	499	12	84
451	G[102]	8481.5	386	12	84
452	G[104]	8469.5	499	12	84
453	G[106]	8456.5	386	12	84
454	G[108]	8444.5	499	12	84
455	G[110]	8431.5	386	12	84
456	G[112]	8419.5	499	12	84
457	G[114]	8406.5	386	12	84
458	G[116]	8394.5	499	12	84
459	G[118]	8381.5	386	12	84
460	G[120]	8369.5	499	12	84
461	G[122]	8356.5	386	12	84
462	G[124]	8344.5	499	12	84
463	G[126]	8331.5	386	12	84
464	G[128]	8319.5	499	12	84
465	G[130]	8306.5	386	12	84
466	G[132]	8294.5	499	12	84
467	G[134]	8281.5	386	12	84
468	G[136]	8269.5	499	12	84
469	G[138]	8256.5	386	12	84
470	G[140]	8244.5	499	12	84
471	G[142]	8231.5	386	12	84
472	G[144]	8219.5	499	12	84
473	G[146]	8206.5	386	12	84
474	G[148]	8194.5	499	12	84
475	G[150]	8181.5	386	12	84
476	G[152]	8169.5	499	12	84
477	G[154]	8156.5	386	12	84
478	G[156]	8144.5	499	12	84
479	G[158]	8131.5	386	12	84
480	G[160]	8119.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
481	G[162]	8106.5	386	12	84
482	G[164]	8094.5	499	12	84
483	G[166]	8081.5	386	12	84
484	G[168]	8069.5	499	12	84
485	G[170]	8056.5	386	12	84
486	G[172]	8044.5	499	12	84
487	G[174]	8031.5	386	12	84
488	G[176]	8019.5	499	12	84
489	G[178]	8006.5	386	12	84
490	G[180]	7994.5	499	12	84
491	G[182]	7981.5	386	12	84
492	G[184]	7969.5	499	12	84
493	G[186]	7956.5	386	12	84
494	G[188]	7944.5	499	12	84
495	G[190]	7931.5	386	12	84
496	G[192]	7919.5	499	12	84
497	G[194]	7906.5	386	12	84
498	G[196]	7894.5	499	12	84
499	G[198]	7881.5	386	12	84
500	G[200]	7869.5	499	12	84
501	G[202]	7856.5	386	12	84
502	G[204]	7844.5	499	12	84
503	G[206]	7831.5	386	12	84
504	G[208]	7819.5	499	12	84
505	G[210]	7806.5	386	12	84
506	G[212]	7794.5	499	12	84
507	G[214]	7781.5	386	12	84
508	G[216]	7769.5	499	12	84
509	G[218]	7756.5	386	12	84
510	G[220]	7744.5	499	12	84
511	G[222]	7731.5	386	12	84
512	G[224]	7719.5	499	12	84
513	G[226]	7706.5	386	12	84
514	G[228]	7694.5	499	12	84
515	G[230]	7681.5	386	12	84
516	G[232]	7669.5	499	12	84
517	G[234]	7656.5	386	12	84
518	G[236]	7644.5	499	12	84
519	G[238]	7631.5	386	12	84
520	G[240]	7619.5	499	12	84
521	G[242]	7606.5	386	12	84
522	G[244]	7594.5	499	12	84
523	G[246]	7581.5	386	12	84
524	G[248]	7569.5	499	12	84
525	G[250]	7556.5	386	12	84
526	G[252]	7544.5	499	12	84
527	G[254]	7531.5	386	12	84
528	G[256]	7519.5	499	12	84
529	G[258]	7506.5	386	12	84
530	G[260]	7494.5	499	12	84
531	G[262]	7481.5	386	12	84
532	G[264]	7469.5	499	12	84
533	G[266]	7456.5	386	12	84
534	G[268]	7444.5	499	12	84
535	G[270]	7431.5	386	12	84
536	G[272]	7419.5	499	12	84
537	G[274]	7406.5	386	12	84
538	G[276]	7394.5	499	12	84
539	G[278]	7381.5	386	12	84
540	G[280]	7369.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
541	G[282]	7356.5	386	12	84
542	G[284]	7344.5	499	12	84
543	G[286]	7331.5	386	12	84
544	G[288]	7319.5	499	12	84
545	G[290]	7306.5	386	12	84
546	G[292]	7294.5	499	12	84
547	G[294]	7281.5	386	12	84
548	G[296]	7269.5	499	12	84
549	G[298]	7256.5	386	12	84
550	G[300]	7244.5	499	12	84
551	G[302]	7231.5	386	12	84
552	G[304]	7219.5	499	12	84
553	G[306]	7206.5	386	12	84
554	G[308]	7194.5	499	12	84
555	G[310]	7181.5	386	12	84
556	G[312]	7169.5	499	12	84
557	G[314]	7156.5	386	12	84
558	G[316]	7144.5	499	12	84
559	G[318]	7131.5	386	12	84
560	G[320]	7119.5	499	12	84
561	G[322]	7106.5	386	12	84
562	G[324]	7094.5	499	12	84
563	G[326]	7081.5	386	12	84
564	G[328]	7069.5	499	12	84
565	G[330]	7056.5	386	12	84
566	G[332]	7044.5	499	12	84
567	G[334]	7031.5	386	12	84
568	G[336]	7019.5	499	12	84
569	G[338]	7006.5	386	12	84
570	G[340]	6994.5	499	12	84
571	G[342]	6981.5	386	12	84
572	G[344]	6969.5	499	12	84
573	G[346]	6956.5	386	12	84
574	G[348]	6944.5	499	12	84
575	G[350]	6931.5	386	12	84
576	G[352]	6919.5	499	12	84
577	G[354]	6906.5	386	12	84
578	G[356]	6894.5	499	12	84
579	G[358]	6881.5	386	12	84
580	G[360]	6869.5	499	12	84
581	G[362]	6856.5	386	12	84
582	G[364]	6844.5	499	12	84
583	G[366]	6831.5	386	12	84
584	G[368]	6819.5	499	12	84
585	G[370]	6806.5	386	12	84
586	G[372]	6794.5	499	12	84
587	G[374]	6781.5	386	12	84
588	G[376]	6769.5	499	12	84
589	G[378]	6756.5	386	12	84
590	G[380]	6744.5	499	12	84
591	G[382]	6731.5	386	12	84
592	G[384]	6719.5	499	12	84
593	G[386]	6706.5	386	12	84
594	G[388]	6694.5	499	12	84
595	G[390]	6681.5	386	12	84
596	G[392]	6669.5	499	12	84
597	G[394]	6656.5	386	12	84
598	G[396]	6644.5	499	12	84
599	G[398]	6631.5	386	12	84
600	G[400]	6619.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
601	G[402]	6606.5	386	12	84
602	G[404]	6594.5	499	12	84
603	G[406]	6581.5	386	12	84
604	G[408]	6569.5	499	12	84
605	G[410]	6556.5	386	12	84
606	G[412]	6544.5	499	12	84
607	G[414]	6531.5	386	12	84
608	G[416]	6519.5	499	12	84
609	G[418]	6506.5	386	12	84
610	G[420]	6494.5	499	12	84
611	G[422]	6481.5	386	12	84
612	G[424]	6469.5	499	12	84
613	G[426]	6456.5	386	12	84
614	G[428]	6444.5	499	12	84
615	G[430]	6431.5	386	12	84
616	G[432]	6419.5	499	12	84
617	G[434]	6406.5	386	12	84
618	G[436]	6394.5	499	12	84
619	G[438]	6381.5	386	12	84
620	G[440]	6369.5	499	12	84
621	G[442]	6356.5	386	12	84
622	G[444]	6344.5	499	12	84
623	G[446]	6331.5	386	12	84
624	G[448]	6319.5	499	12	84
625	G[450]	6306.5	386	12	84
626	G[452]	6294.5	499	12	84
627	G[454]	6281.5	386	12	84
628	G[456]	6269.5	499	12	84
629	G[458]	6256.5	386	12	84
630	G[460]	6244.5	499	12	84
631	G[462]	6231.5	386	12	84
632	G[464]	6219.5	499	12	84
633	G[466]	6206.5	386	12	84
634	G[468]	6194.5	499	12	84
635	G[470]	6181.5	386	12	84
636	G[472]	6169.5	499	12	84
637	G[474]	6156.5	386	12	84
638	G[476]	6144.5	499	12	84
639	G[478]	6131.5	386	12	84
640	G[480]	6119.5	499	12	84
641	G[482]	6106.5	386	12	84
642	G[484]	6094.5	499	12	84
643	G[486]	6081.5	386	12	84
644	G[488]	6069.5	499	12	84
645	G[490]	6056.5	386	12	84
646	G[492]	6044.5	499	12	84
647	G[494]	6031.5	386	12	84
648	G[496]	6019.5	499	12	84
649	G[498]	6006.5	386	12	84
650	G[500]	5994.5	499	12	84
651	G[502]	5981.5	386	12	84
652	G[504]	5969.5	499	12	84
653	G[506]	5956.5	386	12	84
654	G[508]	5944.5	499	12	84
655	G[510]	5931.5	386	12	84
656	G[512]	5919.5	499	12	84
657	G[514]	5906.5	386	12	84
658	G[516]	5894.5	499	12	84
659	G[518]	5881.5	386	12	84
660	G[520]	5869.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
661	G[522]	5856.5	386	12	84
662	G[524]	5844.5	499	12	84
663	G[526]	5831.5	386	12	84
664	G[528]	5819.5	499	12	84
665	G[530]	5806.5	386	12	84
666	G[532]	5794.5	499	12	84
667	G[534]	5781.5	386	12	84
668	G[536]	5769.5	499	12	84
669	G[538]	5756.5	386	12	84
670	G[540]	5744.5	499	12	84
671	G[542]	5731.5	386	12	84
672	G[544]	5719.5	499	12	84
673	G[546]	5706.5	386	12	84
674	G[548]	5694.5	499	12	84
675	G[550]	5681.5	386	12	84
676	G[552]	5669.5	499	12	84
677	G[554]	5656.5	386	12	84
678	G[556]	5644.5	499	12	84
679	G[558]	5631.5	386	12	84
680	G[560]	5619.5	499	12	84
681	G[562]	5606.5	386	12	84
682	G[564]	5594.5	499	12	84
683	G[566]	5581.5	386	12	84
684	G[568]	5569.5	499	12	84
685	G[570]	5556.5	386	12	84
686	G[572]	5544.5	499	12	84
687	G[574]	5531.5	386	12	84
688	G[576]	5519.5	499	12	84
689	G[578]	5506.5	386	12	84
690	G[580]	5494.5	499	12	84
691	G[582]	5481.5	386	12	84
692	G[584]	5469.5	499	12	84
693	G[586]	5456.5	386	12	84
694	G[588]	5444.5	499	12	84
695	G[590]	5431.5	386	12	84
696	G[592]	5419.5	499	12	84
697	G[594]	5406.5	386	12	84
698	G[596]	5394.5	499	12	84
699	G[598]	5381.5	386	12	84
700	DUMMY[99]	5369.5	499	12	84
701	DUMMY[100]	5356.5	386	12	84
702	DUMMY[101]	5344.5	499	12	84
703	DUMMY[102]	5331.5	386	12	84
704	DUMMY[103]	5232.5	499	12	84
705	DUMMY[104]	5219.5	386	12	84
706	VBD[1]	5206.5	499	12	84
707	S[0]	5193.5	386	12	84
708	S[1]	5180.5	499	12	84
709	S[2]	5167.5	386	12	84
710	S[3]	5154.5	499	12	84
711	S[4]	5141.5	386	12	84
712	S[5]	5128.5	499	12	84
713	S[6]	5115.5	386	12	84
714	S[7]	5102.5	499	12	84
715	S[8]	5089.5	386	12	84
716	S[9]	5076.5	499	12	84
717	S[10]	5063.5	386	12	84
718	S[11]	5050.5	499	12	84
719	S[12]	5037.5	386	12	84
720	S[13]	5024.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
721	S[14]	5011.5	386	12	84
722	S[15]	4998.5	499	12	84
723	S[16]	4985.5	386	12	84
724	S[17]	4972.5	499	12	84
725	S[18]	4959.5	386	12	84
726	S[19]	4946.5	499	12	84
727	S[20]	4933.5	386	12	84
728	S[21]	4920.5	499	12	84
729	S[22]	4907.5	386	12	84
730	S[23]	4894.5	499	12	84
731	S[24]	4881.5	386	12	84
732	S[25]	4868.5	499	12	84
733	S[26]	4855.5	386	12	84
734	S[27]	4842.5	499	12	84
735	S[28]	4829.5	386	12	84
736	S[29]	4816.5	499	12	84
737	S[30]	4803.5	386	12	84
738	S[31]	4790.5	499	12	84
739	S[32]	4777.5	386	12	84
740	S[33]	4764.5	499	12	84
741	S[34]	4751.5	386	12	84
742	S[35]	4738.5	499	12	84
743	S[36]	4725.5	386	12	84
744	S[37]	4712.5	499	12	84
745	S[38]	4699.5	386	12	84
746	S[39]	4686.5	499	12	84
747	S[40]	4673.5	386	12	84
748	S[41]	4660.5	499	12	84
749	S[42]	4647.5	386	12	84
750	S[43]	4634.5	499	12	84
751	S[44]	4621.5	386	12	84
752	S[45]	4608.5	499	12	84
753	S[46]	4595.5	386	12	84
754	S[47]	4582.5	499	12	84
755	S[48]	4569.5	386	12	84
756	S[49]	4556.5	499	12	84
757	S[50]	4543.5	386	12	84
758	S[51]	4530.5	499	12	84
759	S[52]	4517.5	386	12	84
760	S[53]	4504.5	499	12	84
761	S[54]	4491.5	386	12	84
762	S[55]	4478.5	499	12	84
763	S[56]	4465.5	386	12	84
764	S[57]	4452.5	499	12	84
765	S[58]	4439.5	386	12	84
766	S[59]	4426.5	499	12	84
767	S[60]	4413.5	386	12	84
768	S[61]	4400.5	499	12	84
769	S[62]	4387.5	386	12	84
770	S[63]	4374.5	499	12	84
771	S[64]	4361.5	386	12	84
772	S[65]	4348.5	499	12	84
773	S[66]	4335.5	386	12	84
774	S[67]	4322.5	499	12	84
775	S[68]	4309.5	386	12	84
776	S[69]	4296.5	499	12	84
777	S[70]	4283.5	386	12	84
778	S[71]	4270.5	499	12	84
779	S[72]	4257.5	386	12	84
780	S[73]	4244.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
781	S[74]	4231.5	386	12	84
782	S[75]	4218.5	499	12	84
783	S[76]	4205.5	386	12	84
784	S[77]	4192.5	499	12	84
785	S[78]	4179.5	386	12	84
786	S[79]	4166.5	499	12	84
787	S[80]	4153.5	386	12	84
788	S[81]	4140.5	499	12	84
789	S[82]	4127.5	386	12	84
790	S[83]	4114.5	499	12	84
791	S[84]	4101.5	386	12	84
792	S[85]	4088.5	499	12	84
793	S[86]	4075.5	386	12	84
794	S[87]	4062.5	499	12	84
795	S[88]	4049.5	386	12	84
796	S[89]	4036.5	499	12	84
797	S[90]	4023.5	386	12	84
798	S[91]	4010.5	499	12	84
799	S[92]	3997.5	386	12	84
800	S[93]	3984.5	499	12	84
801	S[94]	3971.5	386	12	84
802	S[95]	3958.5	499	12	84
803	S[96]	3945.5	386	12	84
804	S[97]	3932.5	499	12	84
805	S[98]	3919.5	386	12	84
806	S[99]	3906.5	499	12	84
807	S[100]	3893.5	386	12	84
808	S[101]	3880.5	499	12	84
809	S[102]	3867.5	386	12	84
810	S[103]	3854.5	499	12	84
811	S[104]	3841.5	386	12	84
812	S[105]	3828.5	499	12	84
813	S[106]	3815.5	386	12	84
814	S[107]	3802.5	499	12	84
815	S[108]	3789.5	386	12	84
816	S[109]	3776.5	499	12	84
817	S[110]	3763.5	386	12	84
818	S[111]	3750.5	499	12	84
819	S[112]	3737.5	386	12	84
820	S[113]	3724.5	499	12	84
821	S[114]	3711.5	386	12	84
822	S[115]	3698.5	499	12	84
823	S[116]	3685.5	386	12	84
824	S[117]	3672.5	499	12	84
825	S[118]	3659.5	386	12	84
826	S[119]	3646.5	499	12	84
827	S[120]	3633.5	386	12	84
828	S[121]	3620.5	499	12	84
829	S[122]	3607.5	386	12	84
830	S[123]	3594.5	499	12	84
831	S[124]	3581.5	386	12	84
832	S[125]	3568.5	499	12	84
833	S[126]	3555.5	386	12	84
834	S[127]	3542.5	499	12	84
835	S[128]	3529.5	386	12	84
836	S[129]	3516.5	499	12	84
837	S[130]	3503.5	386	12	84
838	S[131]	3490.5	499	12	84
839	S[132]	3477.5	386	12	84
840	S[133]	3464.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
841	S[134]	3451.5	386	12	84
842	S[135]	3438.5	499	12	84
843	S[136]	3425.5	386	12	84
844	S[137]	3412.5	499	12	84
845	S[138]	3399.5	386	12	84
846	S[139]	3386.5	499	12	84
847	S[140]	3373.5	386	12	84
848	S[141]	3360.5	499	12	84
849	S[142]	3347.5	386	12	84
850	S[143]	3334.5	499	12	84
851	S[144]	3321.5	386	12	84
852	S[145]	3308.5	499	12	84
853	S[146]	3295.5	386	12	84
854	S[147]	3282.5	499	12	84
855	S[148]	3269.5	386	12	84
856	S[149]	3256.5	499	12	84
857	S[150]	3243.5	386	12	84
858	S[151]	3230.5	499	12	84
859	S[152]	3217.5	386	12	84
860	S[153]	3204.5	499	12	84
861	S[154]	3191.5	386	12	84
862	S[155]	3178.5	499	12	84
863	S[156]	3165.5	386	12	84
864	S[157]	3152.5	499	12	84
865	S[158]	3139.5	386	12	84
866	S[159]	3126.5	499	12	84
867	S[160]	3113.5	386	12	84
868	S[161]	3100.5	499	12	84
869	S[162]	3087.5	386	12	84
870	S[163]	3074.5	499	12	84
871	S[164]	3061.5	386	12	84
872	S[165]	3048.5	499	12	84
873	S[166]	3035.5	386	12	84
874	S[167]	3022.5	499	12	84
875	S[168]	3009.5	386	12	84
876	S[169]	2996.5	499	12	84
877	S[170]	2983.5	386	12	84
878	S[171]	2970.5	499	12	84
879	S[172]	2957.5	386	12	84
880	S[173]	2944.5	499	12	84
881	S[174]	2931.5	386	12	84
882	S[175]	2918.5	499	12	84
883	S[176]	2905.5	386	12	84
884	S[177]	2892.5	499	12	84
885	S[178]	2879.5	386	12	84
886	S[179]	2866.5	499	12	84
887	S[180]	2853.5	386	12	84
888	S[181]	2840.5	499	12	84
889	S[182]	2827.5	386	12	84
890	S[183]	2814.5	499	12	84
891	S[184]	2801.5	386	12	84
892	S[185]	2788.5	499	12	84
893	S[186]	2775.5	386	12	84
894	S[187]	2762.5	499	12	84
895	S[188]	2749.5	386	12	84
896	S[189]	2736.5	499	12	84
897	S[190]	2723.5	386	12	84
898	S[191]	2710.5	499	12	84
899	S[192]	2697.5	386	12	84
900	S[193]	2684.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
901	S[194]	2671.5	386	12	84
902	S[195]	2658.5	499	12	84
903	S[196]	2645.5	386	12	84
904	S[197]	2632.5	499	12	84
905	S[198]	2619.5	386	12	84
906	S[199]	2606.5	499	12	84
907	S[200]	2593.5	386	12	84
908	S[201]	2580.5	499	12	84
909	S[202]	2567.5	386	12	84
910	S[203]	2554.5	499	12	84
911	S[204]	2541.5	386	12	84
912	S[205]	2528.5	499	12	84
913	S[206]	2515.5	386	12	84
914	S[207]	2502.5	499	12	84
915	S[208]	2489.5	386	12	84
916	S[209]	2476.5	499	12	84
917	S[210]	2463.5	386	12	84
918	S[211]	2450.5	499	12	84
919	S[212]	2437.5	386	12	84
920	S[213]	2424.5	499	12	84
921	S[214]	2411.5	386	12	84
922	S[215]	2398.5	499	12	84
923	S[216]	2385.5	386	12	84
924	S[217]	2372.5	499	12	84
925	S[218]	2359.5	386	12	84
926	S[219]	2346.5	499	12	84
927	S[220]	2333.5	386	12	84
928	S[221]	2320.5	499	12	84
929	S[222]	2307.5	386	12	84
930	S[223]	2294.5	499	12	84
931	S[224]	2281.5	386	12	84
932	S[225]	2268.5	499	12	84
933	S[226]	2255.5	386	12	84
934	S[227]	2242.5	499	12	84
935	S[228]	2229.5	386	12	84
936	S[229]	2216.5	499	12	84
937	S[230]	2203.5	386	12	84
938	S[231]	2190.5	499	12	84
939	S[232]	2177.5	386	12	84
940	S[233]	2164.5	499	12	84
941	S[234]	2151.5	386	12	84
942	S[235]	2138.5	499	12	84
943	S[236]	2125.5	386	12	84
944	S[237]	2112.5	499	12	84
945	S[238]	2099.5	386	12	84
946	S[239]	2086.5	499	12	84
947	S[240]	2073.5	386	12	84
948	S[241]	2060.5	499	12	84
949	S[242]	2047.5	386	12	84
950	S[243]	2034.5	499	12	84
951	S[244]	2021.5	386	12	84
952	S[245]	2008.5	499	12	84
953	S[246]	1995.5	386	12	84
954	S[247]	1982.5	499	12	84
955	S[248]	1969.5	386	12	84
956	S[249]	1956.5	499	12	84
957	S[250]	1943.5	386	12	84
958	S[251]	1930.5	499	12	84
959	S[252]	1917.5	386	12	84
960	S[253]	1904.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
961	S[254]	1891.5	386	12	84
962	S[255]	1878.5	499	12	84
963	S[256]	1865.5	386	12	84
964	S[257]	1852.5	499	12	84
965	S[258]	1839.5	386	12	84
966	S[259]	1826.5	499	12	84
967	S[260]	1813.5	386	12	84
968	S[261]	1800.5	499	12	84
969	S[262]	1787.5	386	12	84
970	S[263]	1774.5	499	12	84
971	S[264]	1761.5	386	12	84
972	S[265]	1748.5	499	12	84
973	S[266]	1735.5	386	12	84
974	S[267]	1722.5	499	12	84
975	S[268]	1709.5	386	12	84
976	S[269]	1696.5	499	12	84
977	S[270]	1683.5	386	12	84
978	S[271]	1670.5	499	12	84
979	S[272]	1657.5	386	12	84
980	S[273]	1644.5	499	12	84
981	S[274]	1631.5	386	12	84
982	S[275]	1618.5	499	12	84
983	S[276]	1605.5	386	12	84
984	S[277]	1592.5	499	12	84
985	S[278]	1579.5	386	12	84
986	S[279]	1566.5	499	12	84
987	S[280]	1553.5	386	12	84
988	S[281]	1540.5	499	12	84
989	S[282]	1527.5	386	12	84
990	S[283]	1514.5	499	12	84
991	S[284]	1501.5	386	12	84
992	S[285]	1488.5	499	12	84
993	S[286]	1475.5	386	12	84
994	S[287]	1462.5	499	12	84
995	S[288]	1449.5	386	12	84
996	S[289]	1436.5	499	12	84
997	S[290]	1423.5	386	12	84
998	S[291]	1410.5	499	12	84
999	S[292]	1397.5	386	12	84
1000	S[293]	1384.5	499	12	84
1001	S[294]	1371.5	386	12	84
1002	S[295]	1358.5	499	12	84
1003	S[296]	1345.5	386	12	84
1004	S[297]	1332.5	499	12	84
1005	S[298]	1319.5	386	12	84
1006	S[299]	1306.5	499	12	84
1007	S[300]	1293.5	386	12	84
1008	S[301]	1280.5	499	12	84
1009	S[302]	1267.5	386	12	84
1010	S[303]	1254.5	499	12	84
1011	S[304]	1241.5	386	12	84
1012	S[305]	1228.5	499	12	84
1013	S[306]	1215.5	386	12	84
1014	S[307]	1202.5	499	12	84
1015	S[308]	1189.5	386	12	84
1016	S[309]	1176.5	499	12	84
1017	S[310]	1163.5	386	12	84
1018	S[311]	1150.5	499	12	84
1019	S[312]	1137.5	386	12	84
1020	S[313]	1124.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1021	S[314]	1111.5	386	12	84
1022	S[315]	1098.5	499	12	84
1023	S[316]	1085.5	386	12	84
1024	S[317]	1072.5	499	12	84
1025	S[318]	1059.5	386	12	84
1026	S[319]	1046.5	499	12	84
1027	S[320]	1033.5	386	12	84
1028	S[321]	1020.5	499	12	84
1029	S[322]	1007.5	386	12	84
1030	S[323]	994.5	499	12	84
1031	S[324]	981.5	386	12	84
1032	S[325]	968.5	499	12	84
1033	S[326]	955.5	386	12	84
1034	S[327]	942.5	499	12	84
1035	S[328]	929.5	386	12	84
1036	S[329]	916.5	499	12	84
1037	S[330]	903.5	386	12	84
1038	S[331]	890.5	499	12	84
1039	S[332]	877.5	386	12	84
1040	S[333]	864.5	499	12	84
1041	S[334]	851.5	386	12	84
1042	S[335]	838.5	499	12	84
1043	S[336]	825.5	386	12	84
1044	S[337]	812.5	499	12	84
1045	S[338]	799.5	386	12	84
1046	S[339]	786.5	499	12	84
1047	S[340]	773.5	386	12	84
1048	S[341]	760.5	499	12	84
1049	S[342]	747.5	386	12	84
1050	S[343]	734.5	499	12	84
1051	S[344]	721.5	386	12	84
1052	S[345]	708.5	499	12	84
1053	S[346]	695.5	386	12	84
1054	S[347]	682.5	499	12	84
1055	S[348]	669.5	386	12	84
1056	S[349]	656.5	499	12	84
1057	S[350]	643.5	386	12	84
1058	S[351]	630.5	499	12	84
1059	S[352]	617.5	386	12	84
1060	S[353]	604.5	499	12	84
1061	S[354]	591.5	386	12	84
1062	S[355]	578.5	499	12	84
1063	S[356]	565.5	386	12	84
1064	S[357]	552.5	499	12	84
1065	S[358]	539.5	386	12	84
1066	S[359]	526.5	499	12	84
1067	S[360]	513.5	386	12	84
1068	S[361]	500.5	499	12	84
1069	S[362]	487.5	386	12	84
1070	S[363]	474.5	499	12	84
1071	S[364]	461.5	386	12	84
1072	S[365]	448.5	499	12	84
1073	S[366]	435.5	386	12	84
1074	S[367]	422.5	499	12	84
1075	S[368]	409.5	386	12	84
1076	S[369]	396.5	499	12	84
1077	S[370]	383.5	386	12	84
1078	S[371]	370.5	499	12	84
1079	S[372]	357.5	386	12	84
1080	S[373]	344.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1081	S[374]	331.5	386	12	84
1082	S[375]	318.5	499	12	84
1083	S[376]	305.5	386	12	84
1084	S[377]	292.5	499	12	84
1085	S[378]	279.5	386	12	84
1086	S[379]	266.5	499	12	84
1087	S[380]	253.5	386	12	84
1088	S[381]	240.5	499	12	84
1089	S[382]	227.5	386	12	84
1090	S[383]	214.5	499	12	84
1091	S[384]	201.5	386	12	84
1092	S[385]	188.5	499	12	84
1093	S[386]	175.5	386	12	84
1094	S[387]	162.5	499	12	84
1095	S[388]	149.5	386	12	84
1096	S[389]	136.5	499	12	84
1097	S[390]	123.5	386	12	84
1098	S[391]	110.5	499	12	84
1099	S[392]	97.5	386	12	84
1100	S[393]	84.5	499	12	84
1101	S[394]	71.5	386	12	84
1102	S[395]	58.5	499	12	84
1103	S[396]	45.5	386	12	84
1104	S[397]	32.5	499	12	84
1105	S[398]	19.5	386	12	84
1106	S[399]	6.5	499	12	84
1107	S[400]	-6.5	386	12	84
1108	S[401]	-19.5	499	12	84
1109	S[402]	-32.5	386	12	84
1110	S[403]	-45.5	499	12	84
1111	S[404]	-58.5	386	12	84
1112	S[405]	-71.5	499	12	84
1113	S[406]	-84.5	386	12	84
1114	S[407]	-97.5	499	12	84
1115	S[408]	-110.5	386	12	84
1116	S[409]	-123.5	499	12	84
1117	S[410]	-136.5	386	12	84
1118	S[411]	-149.5	499	12	84
1119	S[412]	-162.5	386	12	84
1120	S[413]	-175.5	499	12	84
1121	S[414]	-188.5	386	12	84
1122	S[415]	-201.5	499	12	84
1123	S[416]	-214.5	386	12	84
1124	S[417]	-227.5	499	12	84
1125	S[418]	-240.5	386	12	84
1126	S[419]	-253.5	499	12	84
1127	S[420]	-266.5	386	12	84
1128	S[421]	-279.5	499	12	84
1129	S[422]	-292.5	386	12	84
1130	S[423]	-305.5	499	12	84
1131	S[424]	-318.5	386	12	84
1132	S[425]	-331.5	499	12	84
1133	S[426]	-344.5	386	12	84
1134	S[427]	-357.5	499	12	84
1135	S[428]	-370.5	386	12	84
1136	S[429]	-383.5	499	12	84
1137	S[430]	-396.5	386	12	84
1138	S[431]	-409.5	499	12	84
1139	S[432]	-422.5	386	12	84
1140	S[433]	-435.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1141	S[434]	-448.5	386	12	84
1142	S[435]	-461.5	499	12	84
1143	S[436]	-474.5	386	12	84
1144	S[437]	-487.5	499	12	84
1145	S[438]	-500.5	386	12	84
1146	S[439]	-513.5	499	12	84
1147	S[440]	-526.5	386	12	84
1148	S[441]	-539.5	499	12	84
1149	S[442]	-552.5	386	12	84
1150	S[443]	-565.5	499	12	84
1151	S[444]	-578.5	386	12	84
1152	S[445]	-591.5	499	12	84
1153	S[446]	-604.5	386	12	84
1154	S[447]	-617.5	499	12	84
1155	S[448]	-630.5	386	12	84
1156	S[449]	-643.5	499	12	84
1157	S[450]	-656.5	386	12	84
1158	S[451]	-669.5	499	12	84
1159	S[452]	-682.5	386	12	84
1160	S[453]	-695.5	499	12	84
1161	S[454]	-708.5	386	12	84
1162	S[455]	-721.5	499	12	84
1163	S[456]	-734.5	386	12	84
1164	S[457]	-747.5	499	12	84
1165	S[458]	-760.5	386	12	84
1166	S[459]	-773.5	499	12	84
1167	S[460]	-786.5	386	12	84
1168	S[461]	-799.5	499	12	84
1169	S[462]	-812.5	386	12	84
1170	S[463]	-825.5	499	12	84
1171	S[464]	-838.5	386	12	84
1172	S[465]	-851.5	499	12	84
1173	S[466]	-864.5	386	12	84
1174	S[467]	-877.5	499	12	84
1175	S[468]	-890.5	386	12	84
1176	S[469]	-903.5	499	12	84
1177	S[470]	-916.5	386	12	84
1178	S[471]	-929.5	499	12	84
1179	S[472]	-942.5	386	12	84
1180	S[473]	-955.5	499	12	84
1181	S[474]	-968.5	386	12	84
1182	S[475]	-981.5	499	12	84
1183	S[476]	-994.5	386	12	84
1184	S[477]	-1007.5	499	12	84
1185	S[478]	-1020.5	386	12	84
1186	S[479]	-1033.5	499	12	84
1187	S[480]	-1046.5	386	12	84
1188	S[481]	-1059.5	499	12	84
1189	S[482]	-1072.5	386	12	84
1190	S[483]	-1085.5	499	12	84
1191	S[484]	-1098.5	386	12	84
1192	S[485]	-1111.5	499	12	84
1193	S[486]	-1124.5	386	12	84
1194	S[487]	-1137.5	499	12	84
1195	S[488]	-1150.5	386	12	84
1196	S[489]	-1163.5	499	12	84
1197	S[490]	-1176.5	386	12	84
1198	S[491]	-1189.5	499	12	84
1199	S[492]	-1202.5	386	12	84
1200	S[493]	-1215.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1201	S[494]	-1228.5	386	12	84
1202	S[495]	-1241.5	499	12	84
1203	S[496]	-1254.5	386	12	84
1204	S[497]	-1267.5	499	12	84
1205	S[498]	-1280.5	386	12	84
1206	S[499]	-1293.5	499	12	84
1207	S[500]	-1306.5	386	12	84
1208	S[501]	-1319.5	499	12	84
1209	S[502]	-1332.5	386	12	84
1210	S[503]	-1345.5	499	12	84
1211	S[504]	-1358.5	386	12	84
1212	S[505]	-1371.5	499	12	84
1213	S[506]	-1384.5	386	12	84
1214	S[507]	-1397.5	499	12	84
1215	S[508]	-1410.5	386	12	84
1216	S[509]	-1423.5	499	12	84
1217	S[510]	-1436.5	386	12	84
1218	S[511]	-1449.5	499	12	84
1219	S[512]	-1462.5	386	12	84
1220	S[513]	-1475.5	499	12	84
1221	S[514]	-1488.5	386	12	84
1222	S[515]	-1501.5	499	12	84
1223	S[516]	-1514.5	386	12	84
1224	S[517]	-1527.5	499	12	84
1225	S[518]	-1540.5	386	12	84
1226	S[519]	-1553.5	499	12	84
1227	S[520]	-1566.5	386	12	84
1228	S[521]	-1579.5	499	12	84
1229	S[522]	-1592.5	386	12	84
1230	S[523]	-1605.5	499	12	84
1231	S[524]	-1618.5	386	12	84
1232	S[525]	-1631.5	499	12	84
1233	S[526]	-1644.5	386	12	84
1234	S[527]	-1657.5	499	12	84
1235	S[528]	-1670.5	386	12	84
1236	S[529]	-1683.5	499	12	84
1237	S[530]	-1696.5	386	12	84
1238	S[531]	-1709.5	499	12	84
1239	S[532]	-1722.5	386	12	84
1240	S[533]	-1735.5	499	12	84
1241	S[534]	-1748.5	386	12	84
1242	S[535]	-1761.5	499	12	84
1243	S[536]	-1774.5	386	12	84
1244	S[537]	-1787.5	499	12	84
1245	S[538]	-1800.5	386	12	84
1246	S[539]	-1813.5	499	12	84
1247	S[540]	-1826.5	386	12	84
1248	S[541]	-1839.5	499	12	84
1249	S[542]	-1852.5	386	12	84
1250	S[543]	-1865.5	499	12	84
1251	S[544]	-1878.5	386	12	84
1252	S[545]	-1891.5	499	12	84
1253	S[546]	-1904.5	386	12	84
1254	S[547]	-1917.5	499	12	84
1255	S[548]	-1930.5	386	12	84
1256	S[549]	-1943.5	499	12	84
1257	S[550]	-1956.5	386	12	84
1258	S[551]	-1969.5	499	12	84
1259	S[552]	-1982.5	386	12	84
1260	S[553]	-1995.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1261	S[554]	-2008.5	386	12	84
1262	S[555]	-2021.5	499	12	84
1263	S[556]	-2034.5	386	12	84
1264	S[557]	-2047.5	499	12	84
1265	S[558]	-2060.5	386	12	84
1266	S[559]	-2073.5	499	12	84
1267	S[560]	-2086.5	386	12	84
1268	S[561]	-2099.5	499	12	84
1269	S[562]	-2112.5	386	12	84
1270	S[563]	-2125.5	499	12	84
1271	S[564]	-2138.5	386	12	84
1272	S[565]	-2151.5	499	12	84
1273	S[566]	-2164.5	386	12	84
1274	S[567]	-2177.5	499	12	84
1275	S[568]	-2190.5	386	12	84
1276	S[569]	-2203.5	499	12	84
1277	S[570]	-2216.5	386	12	84
1278	S[571]	-2229.5	499	12	84
1279	S[572]	-2242.5	386	12	84
1280	S[573]	-2255.5	499	12	84
1281	S[574]	-2268.5	386	12	84
1282	S[575]	-2281.5	499	12	84
1283	S[576]	-2294.5	386	12	84
1284	S[577]	-2307.5	499	12	84
1285	S[578]	-2320.5	386	12	84
1286	S[579]	-2333.5	499	12	84
1287	S[580]	-2346.5	386	12	84
1288	S[581]	-2359.5	499	12	84
1289	S[582]	-2372.5	386	12	84
1290	S[583]	-2385.5	499	12	84
1291	S[584]	-2398.5	386	12	84
1292	S[585]	-2411.5	499	12	84
1293	S[586]	-2424.5	386	12	84
1294	S[587]	-2437.5	499	12	84
1295	S[588]	-2450.5	386	12	84
1296	S[589]	-2463.5	499	12	84
1297	S[590]	-2476.5	386	12	84
1298	S[591]	-2489.5	499	12	84
1299	S[592]	-2502.5	386	12	84
1300	S[593]	-2515.5	499	12	84
1301	S[594]	-2528.5	386	12	84
1302	S[595]	-2541.5	499	12	84
1303	S[596]	-2554.5	386	12	84
1304	S[597]	-2567.5	499	12	84
1305	S[598]	-2580.5	386	12	84
1306	S[599]	-2593.5	499	12	84
1307	S[600]	-2606.5	386	12	84
1308	S[601]	-2619.5	499	12	84
1309	S[602]	-2632.5	386	12	84
1310	S[603]	-2645.5	499	12	84
1311	S[604]	-2658.5	386	12	84
1312	S[605]	-2671.5	499	12	84
1313	S[606]	-2684.5	386	12	84
1314	S[607]	-2697.5	499	12	84
1315	S[608]	-2710.5	386	12	84
1316	S[609]	-2723.5	499	12	84
1317	S[610]	-2736.5	386	12	84
1318	S[611]	-2749.5	499	12	84
1319	S[612]	-2762.5	386	12	84
1320	S[613]	-2775.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1321	S[614]	-2788.5	386	12	84
1322	S[615]	-2801.5	499	12	84
1323	S[616]	-2814.5	386	12	84
1324	S[617]	-2827.5	499	12	84
1325	S[618]	-2840.5	386	12	84
1326	S[619]	-2853.5	499	12	84
1327	S[620]	-2866.5	386	12	84
1328	S[621]	-2879.5	499	12	84
1329	S[622]	-2892.5	386	12	84
1330	S[623]	-2905.5	499	12	84
1331	S[624]	-2918.5	386	12	84
1332	S[625]	-2931.5	499	12	84
1333	S[626]	-2944.5	386	12	84
1334	S[627]	-2957.5	499	12	84
1335	S[628]	-2970.5	386	12	84
1336	S[629]	-2983.5	499	12	84
1337	S[630]	-2996.5	386	12	84
1338	S[631]	-3009.5	499	12	84
1339	S[632]	-3022.5	386	12	84
1340	S[633]	-3035.5	499	12	84
1341	S[634]	-3048.5	386	12	84
1342	S[635]	-3061.5	499	12	84
1343	S[636]	-3074.5	386	12	84
1344	S[637]	-3087.5	499	12	84
1345	S[638]	-3100.5	386	12	84
1346	S[639]	-3113.5	499	12	84
1347	S[640]	-3126.5	386	12	84
1348	S[641]	-3139.5	499	12	84
1349	S[642]	-3152.5	386	12	84
1350	S[643]	-3165.5	499	12	84
1351	S[644]	-3178.5	386	12	84
1352	S[645]	-3191.5	499	12	84
1353	S[646]	-3204.5	386	12	84
1354	S[647]	-3217.5	499	12	84
1355	S[648]	-3230.5	386	12	84
1356	S[649]	-3243.5	499	12	84
1357	S[650]	-3256.5	386	12	84
1358	S[651]	-3269.5	499	12	84
1359	S[652]	-3282.5	386	12	84
1360	S[653]	-3295.5	499	12	84
1361	S[654]	-3308.5	386	12	84
1362	S[655]	-3321.5	499	12	84
1363	S[656]	-3334.5	386	12	84
1364	S[657]	-3347.5	499	12	84
1365	S[658]	-3360.5	386	12	84
1366	S[659]	-3373.5	499	12	84
1367	S[660]	-3386.5	386	12	84
1368	S[661]	-3399.5	499	12	84
1369	S[662]	-3412.5	386	12	84
1370	S[663]	-3425.5	499	12	84
1371	S[664]	-3438.5	386	12	84
1372	S[665]	-3451.5	499	12	84
1373	S[666]	-3464.5	386	12	84
1374	S[667]	-3477.5	499	12	84
1375	S[668]	-3490.5	386	12	84
1376	S[669]	-3503.5	499	12	84
1377	S[670]	-3516.5	386	12	84
1378	S[671]	-3529.5	499	12	84
1379	S[672]	-3542.5	386	12	84
1380	S[673]	-3555.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1381	S[674]	-3568.5	386	12	84
1382	S[675]	-3581.5	499	12	84
1383	S[676]	-3594.5	386	12	84
1384	S[677]	-3607.5	499	12	84
1385	S[678]	-3620.5	386	12	84
1386	S[679]	-3633.5	499	12	84
1387	S[680]	-3646.5	386	12	84
1388	S[681]	-3659.5	499	12	84
1389	S[682]	-3672.5	386	12	84
1390	S[683]	-3685.5	499	12	84
1391	S[684]	-3698.5	386	12	84
1392	S[685]	-3711.5	499	12	84
1393	S[686]	-3724.5	386	12	84
1394	S[687]	-3737.5	499	12	84
1395	S[688]	-3750.5	386	12	84
1396	S[689]	-3763.5	499	12	84
1397	S[690]	-3776.5	386	12	84
1398	S[691]	-3789.5	499	12	84
1399	S[692]	-3802.5	386	12	84
1400	S[693]	-3815.5	499	12	84
1401	S[694]	-3828.5	386	12	84
1402	S[695]	-3841.5	499	12	84
1403	S[696]	-3854.5	386	12	84
1404	S[697]	-3867.5	499	12	84
1405	S[698]	-3880.5	386	12	84
1406	S[699]	-3893.5	499	12	84
1407	S[700]	-3906.5	386	12	84
1408	S[701]	-3919.5	499	12	84
1409	S[702]	-3932.5	386	12	84
1410	S[703]	-3945.5	499	12	84
1411	S[704]	-3958.5	386	12	84
1412	S[705]	-3971.5	499	12	84
1413	S[706]	-3984.5	386	12	84
1414	S[707]	-3997.5	499	12	84
1415	S[708]	-4010.5	386	12	84
1416	S[709]	-4023.5	499	12	84
1417	S[710]	-4036.5	386	12	84
1418	S[711]	-4049.5	499	12	84
1419	S[712]	-4062.5	386	12	84
1420	S[713]	-4075.5	499	12	84
1421	S[714]	-4088.5	386	12	84
1422	S[715]	-4101.5	499	12	84
1423	S[716]	-4114.5	386	12	84
1424	S[717]	-4127.5	499	12	84
1425	S[718]	-4140.5	386	12	84
1426	S[719]	-4153.5	499	12	84
1427	S[720]	-4166.5	386	12	84
1428	S[721]	-4179.5	499	12	84
1429	S[722]	-4192.5	386	12	84
1430	S[723]	-4205.5	499	12	84
1431	S[724]	-4218.5	386	12	84
1432	S[725]	-4231.5	499	12	84
1433	S[726]	-4244.5	386	12	84
1434	S[727]	-4257.5	499	12	84
1435	S[728]	-4270.5	386	12	84
1436	S[729]	-4283.5	499	12	84
1437	S[730]	-4296.5	386	12	84
1438	S[731]	-4309.5	499	12	84
1439	S[732]	-4322.5	386	12	84
1440	S[733]	-4335.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1441	S[734]	-4348.5	386	12	84
1442	S[735]	-4361.5	499	12	84
1443	S[736]	-4374.5	386	12	84
1444	S[737]	-4387.5	499	12	84
1445	S[738]	-4400.5	386	12	84
1446	S[739]	-4413.5	499	12	84
1447	S[740]	-4426.5	386	12	84
1448	S[741]	-4439.5	499	12	84
1449	S[742]	-4452.5	386	12	84
1450	S[743]	-4465.5	499	12	84
1451	S[744]	-4478.5	386	12	84
1452	S[745]	-4491.5	499	12	84
1453	S[746]	-4504.5	386	12	84
1454	S[747]	-4517.5	499	12	84
1455	S[748]	-4530.5	386	12	84
1456	S[749]	-4543.5	499	12	84
1457	S[750]	-4556.5	386	12	84
1458	S[751]	-4569.5	499	12	84
1459	S[752]	-4582.5	386	12	84
1460	S[753]	-4595.5	499	12	84
1461	S[754]	-4608.5	386	12	84
1462	S[755]	-4621.5	499	12	84
1463	S[756]	-4634.5	386	12	84
1464	S[757]	-4647.5	499	12	84
1465	S[758]	-4660.5	386	12	84
1466	S[759]	-4673.5	499	12	84
1467	S[760]	-4686.5	386	12	84
1468	S[761]	-4699.5	499	12	84
1469	S[762]	-4712.5	386	12	84
1470	S[763]	-4725.5	499	12	84
1471	S[764]	-4738.5	386	12	84
1472	S[765]	-4751.5	499	12	84
1473	S[766]	-4764.5	386	12	84
1474	S[767]	-4777.5	499	12	84
1475	S[768]	-4790.5	386	12	84
1476	S[769]	-4803.5	499	12	84
1477	S[770]	-4816.5	386	12	84
1478	S[771]	-4829.5	499	12	84
1479	S[772]	-4842.5	386	12	84
1480	S[773]	-4855.5	499	12	84
1481	S[774]	-4868.5	386	12	84
1482	S[775]	-4881.5	499	12	84
1483	S[776]	-4894.5	386	12	84
1484	S[777]	-4907.5	499	12	84
1485	S[778]	-4920.5	386	12	84
1486	S[779]	-4933.5	499	12	84
1487	S[780]	-4946.5	386	12	84
1488	S[781]	-4959.5	499	12	84
1489	S[782]	-4972.5	386	12	84
1490	S[783]	-4985.5	499	12	84
1491	S[784]	-4998.5	386	12	84
1492	S[785]	-5011.5	499	12	84
1493	S[786]	-5024.5	386	12	84
1494	S[787]	-5037.5	499	12	84
1495	S[788]	-5050.5	386	12	84
1496	S[789]	-5063.5	499	12	84
1497	S[790]	-5076.5	386	12	84
1498	S[791]	-5089.5	499	12	84
1499	S[792]	-5102.5	386	12	84
1500	S[793]	-5115.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1501	S[794]	-5128.5	386	12	84
1502	S[795]	-5141.5	499	12	84
1503	S[796]	-5154.5	386	12	84
1504	S[797]	-5167.5	499	12	84
1505	S[798]	-5180.5	386	12	84
1506	S[799]	-5193.5	499	12	84
1507	VBD[2]	-5206.5	386	12	84
1508	DUMMY[105]	-5219.5	499	12	84
1509	DUMMY[106]	-5232.5	386	12	84
1510	DUMMY[107]	-5331.5	499	12	84
1511	DUMMY[108]	-5344.5	386	12	84
1512	DUMMY[109]	-5356.5	499	12	84
1513	DUMMY[110]	-5369.5	386	12	84
1514	G[599]	-5381.5	499	12	84
1515	G[597]	-5394.5	386	12	84
1516	G[595]	-5406.5	499	12	84
1517	G[593]	-5419.5	386	12	84
1518	G[591]	-5431.5	499	12	84
1519	G[589]	-5444.5	386	12	84
1520	G[587]	-5456.5	499	12	84
1521	G[585]	-5469.5	386	12	84
1522	G[583]	-5481.5	499	12	84
1523	G[581]	-5494.5	386	12	84
1524	G[579]	-5506.5	499	12	84
1525	G[577]	-5519.5	386	12	84
1526	G[575]	-5531.5	499	12	84
1527	G[573]	-5544.5	386	12	84
1528	G[571]	-5556.5	499	12	84
1529	G[569]	-5569.5	386	12	84
1530	G[567]	-5581.5	499	12	84
1531	G[565]	-5594.5	386	12	84
1532	G[563]	-5606.5	499	12	84
1533	G[561]	-5619.5	386	12	84
1534	G[559]	-5631.5	499	12	84
1535	G[557]	-5644.5	386	12	84
1536	G[555]	-5656.5	499	12	84
1537	G[553]	-5669.5	386	12	84
1538	G[551]	-5681.5	499	12	84
1539	G[549]	-5694.5	386	12	84
1540	G[547]	-5706.5	499	12	84
1541	G[545]	-5719.5	386	12	84
1542	G[543]	-5731.5	499	12	84
1543	G[541]	-5744.5	386	12	84
1544	G[539]	-5756.5	499	12	84
1545	G[537]	-5769.5	386	12	84
1546	G[535]	-5781.5	499	12	84
1547	G[533]	-5794.5	386	12	84
1548	G[531]	-5806.5	499	12	84
1549	G[529]	-5819.5	386	12	84
1550	G[527]	-5831.5	499	12	84
1551	G[525]	-5844.5	386	12	84
1552	G[523]	-5856.5	499	12	84
1553	G[521]	-5869.5	386	12	84
1554	G[519]	-5881.5	499	12	84
1555	G[517]	-5894.5	386	12	84
1556	G[515]	-5906.5	499	12	84
1557	G[513]	-5919.5	386	12	84
1558	G[511]	-5931.5	499	12	84
1559	G[509]	-5944.5	386	12	84
1560	G[507]	-5956.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1561	G[505]	-5969.5	386	12	84
1562	G[503]	-5981.5	499	12	84
1563	G[501]	-5994.5	386	12	84
1564	G[499]	-6006.5	499	12	84
1565	G[497]	-6019.5	386	12	84
1566	G[495]	-6031.5	499	12	84
1567	G[493]	-6044.5	386	12	84
1568	G[491]	-6056.5	499	12	84
1569	G[489]	-6069.5	386	12	84
1570	G[487]	-6081.5	499	12	84
1571	G[485]	-6094.5	386	12	84
1572	G[483]	-6106.5	499	12	84
1573	G[481]	-6119.5	386	12	84
1574	G[479]	-6131.5	499	12	84
1575	G[477]	-6144.5	386	12	84
1576	G[475]	-6156.5	499	12	84
1577	G[473]	-6169.5	386	12	84
1578	G[471]	-6181.5	499	12	84
1579	G[469]	-6194.5	386	12	84
1580	G[467]	-6206.5	499	12	84
1581	G[465]	-6219.5	386	12	84
1582	G[463]	-6231.5	499	12	84
1583	G[461]	-6244.5	386	12	84
1584	G[459]	-6256.5	499	12	84
1585	G[457]	-6269.5	386	12	84
1586	G[455]	-6281.5	499	12	84
1587	G[453]	-6294.5	386	12	84
1588	G[451]	-6306.5	499	12	84
1589	G[449]	-6319.5	386	12	84
1590	G[447]	-6331.5	499	12	84
1591	G[445]	-6344.5	386	12	84
1592	G[443]	-6356.5	499	12	84
1593	G[441]	-6369.5	386	12	84
1594	G[439]	-6381.5	499	12	84
1595	G[437]	-6394.5	386	12	84
1596	G[435]	-6406.5	499	12	84
1597	G[433]	-6419.5	386	12	84
1598	G[431]	-6431.5	499	12	84
1599	G[429]	-6444.5	386	12	84
1600	G[427]	-6456.5	499	12	84
1601	G[425]	-6469.5	386	12	84
1602	G[423]	-6481.5	499	12	84
1603	G[421]	-6494.5	386	12	84
1604	G[419]	-6506.5	499	12	84
1605	G[417]	-6519.5	386	12	84
1606	G[415]	-6531.5	499	12	84
1607	G[413]	-6544.5	386	12	84
1608	G[411]	-6556.5	499	12	84
1609	G[409]	-6569.5	386	12	84
1610	G[407]	-6581.5	499	12	84
1611	G[405]	-6594.5	386	12	84
1612	G[403]	-6606.5	499	12	84
1613	G[401]	-6619.5	386	12	84
1614	G[399]	-6631.5	499	12	84
1615	G[397]	-6644.5	386	12	84
1616	G[395]	-6656.5	499	12	84
1617	G[393]	-6669.5	386	12	84
1618	G[391]	-6681.5	499	12	84
1619	G[389]	-6694.5	386	12	84
1620	G[387]	-6706.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1621	G[385]	-6719.5	386	12	84
1622	G[383]	-6731.5	499	12	84
1623	G[381]	-6744.5	386	12	84
1624	G[379]	-6756.5	499	12	84
1625	G[377]	-6769.5	386	12	84
1626	G[375]	-6781.5	499	12	84
1627	G[373]	-6794.5	386	12	84
1628	G[371]	-6806.5	499	12	84
1629	G[369]	-6819.5	386	12	84
1630	G[367]	-6831.5	499	12	84
1631	G[365]	-6844.5	386	12	84
1632	G[363]	-6856.5	499	12	84
1633	G[361]	-6869.5	386	12	84
1634	G[359]	-6881.5	499	12	84
1635	G[357]	-6894.5	386	12	84
1636	G[355]	-6906.5	499	12	84
1637	G[353]	-6919.5	386	12	84
1638	G[351]	-6931.5	499	12	84
1639	G[349]	-6944.5	386	12	84
1640	G[347]	-6956.5	499	12	84
1641	G[345]	-6969.5	386	12	84
1642	G[343]	-6981.5	499	12	84
1643	G[341]	-6994.5	386	12	84
1644	G[339]	-7006.5	499	12	84
1645	G[337]	-7019.5	386	12	84
1646	G[335]	-7031.5	499	12	84
1647	G[333]	-7044.5	386	12	84
1648	G[331]	-7056.5	499	12	84
1649	G[329]	-7069.5	386	12	84
1650	G[327]	-7081.5	499	12	84
1651	G[325]	-7094.5	386	12	84
1652	G[323]	-7106.5	499	12	84
1653	G[321]	-7119.5	386	12	84
1654	G[319]	-7131.5	499	12	84
1655	G[317]	-7144.5	386	12	84
1656	G[315]	-7156.5	499	12	84
1657	G[313]	-7169.5	386	12	84
1658	G[311]	-7181.5	499	12	84
1659	G[309]	-7194.5	386	12	84
1660	G[307]	-7206.5	499	12	84
1661	G[305]	-7219.5	386	12	84
1662	G[303]	-7231.5	499	12	84
1663	G[301]	-7244.5	386	12	84
1664	G[299]	-7256.5	499	12	84
1665	G[297]	-7269.5	386	12	84
1666	G[295]	-7281.5	499	12	84
1667	G[293]	-7294.5	386	12	84
1668	G[291]	-7306.5	499	12	84
1669	G[289]	-7319.5	386	12	84
1670	G[287]	-7331.5	499	12	84
1671	G[285]	-7344.5	386	12	84
1672	G[283]	-7356.5	499	12	84
1673	G[281]	-7369.5	386	12	84
1674	G[279]	-7381.5	499	12	84
1675	G[277]	-7394.5	386	12	84
1676	G[275]	-7406.5	499	12	84
1677	G[273]	-7419.5	386	12	84
1678	G[271]	-7431.5	499	12	84
1679	G[269]	-7444.5	386	12	84
1680	G[267]	-7456.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1681	G[265]	-7469.5	386	12	84
1682	G[263]	-7481.5	499	12	84
1683	G[261]	-7494.5	386	12	84
1684	G[259]	-7506.5	499	12	84
1685	G[257]	-7519.5	386	12	84
1686	G[255]	-7531.5	499	12	84
1687	G[253]	-7544.5	386	12	84
1688	G[251]	-7556.5	499	12	84
1689	G[249]	-7569.5	386	12	84
1690	G[247]	-7581.5	499	12	84
1691	G[245]	-7594.5	386	12	84
1692	G[243]	-7606.5	499	12	84
1693	G[241]	-7619.5	386	12	84
1694	G[239]	-7631.5	499	12	84
1695	G[237]	-7644.5	386	12	84
1696	G[235]	-7656.5	499	12	84
1697	G[233]	-7669.5	386	12	84
1698	G[231]	-7681.5	499	12	84
1699	G[229]	-7694.5	386	12	84
1700	G[227]	-7706.5	499	12	84
1701	G[225]	-7719.5	386	12	84
1702	G[223]	-7731.5	499	12	84
1703	G[221]	-7744.5	386	12	84
1704	G[219]	-7756.5	499	12	84
1705	G[217]	-7769.5	386	12	84
1706	G[215]	-7781.5	499	12	84
1707	G[213]	-7794.5	386	12	84
1708	G[211]	-7806.5	499	12	84
1709	G[209]	-7819.5	386	12	84
1710	G[207]	-7831.5	499	12	84
1711	G[205]	-7844.5	386	12	84
1712	G[203]	-7856.5	499	12	84
1713	G[201]	-7869.5	386	12	84
1714	G[199]	-7881.5	499	12	84
1715	G[197]	-7894.5	386	12	84
1716	G[195]	-7906.5	499	12	84
1717	G[193]	-7919.5	386	12	84
1718	G[191]	-7931.5	499	12	84
1719	G[189]	-7944.5	386	12	84
1720	G[187]	-7956.5	499	12	84
1721	G[185]	-7969.5	386	12	84
1722	G[183]	-7981.5	499	12	84
1723	G[181]	-7994.5	386	12	84
1724	G[179]	-8006.5	499	12	84
1725	G[177]	-8019.5	386	12	84
1726	G[175]	-8031.5	499	12	84
1727	G[173]	-8044.5	386	12	84
1728	G[171]	-8056.5	499	12	84
1729	G[169]	-8069.5	386	12	84
1730	G[167]	-8081.5	499	12	84
1731	G[165]	-8094.5	386	12	84
1732	G[163]	-8106.5	499	12	84
1733	G[161]	-8119.5	386	12	84
1734	G[159]	-8131.5	499	12	84
1735	G[157]	-8144.5	386	12	84
1736	G[155]	-8156.5	499	12	84
1737	G[153]	-8169.5	386	12	84
1738	G[151]	-8181.5	499	12	84
1739	G[149]	-8194.5	386	12	84
1740	G[147]	-8206.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1741	G[145]	-8219.5	386	12	84
1742	G[143]	-8231.5	499	12	84
1743	G[141]	-8244.5	386	12	84
1744	G[139]	-8256.5	499	12	84
1745	G[137]	-8269.5	386	12	84
1746	G[135]	-8281.5	499	12	84
1747	G[133]	-8294.5	386	12	84
1748	G[131]	-8306.5	499	12	84
1749	G[129]	-8319.5	386	12	84
1750	G[127]	-8331.5	499	12	84
1751	G[125]	-8344.5	386	12	84
1752	G[123]	-8356.5	499	12	84
1753	G[121]	-8369.5	386	12	84
1754	G[119]	-8381.5	499	12	84
1755	G[117]	-8394.5	386	12	84
1756	G[115]	-8406.5	499	12	84
1757	G[113]	-8419.5	386	12	84
1758	G[111]	-8431.5	499	12	84
1759	G[109]	-8444.5	386	12	84
1760	G[107]	-8456.5	499	12	84
1761	G[105]	-8469.5	386	12	84
1762	G[103]	-8481.5	499	12	84
1763	G[101]	-8494.5	386	12	84
1764	G[99]	-8506.5	499	12	84
1765	G[97]	-8519.5	386	12	84
1766	G[95]	-8531.5	499	12	84
1767	G[93]	-8544.5	386	12	84
1768	G[91]	-8556.5	499	12	84
1769	G[89]	-8569.5	386	12	84
1770	G[87]	-8581.5	499	12	84
1771	G[85]	-8594.5	386	12	84
1772	G[83]	-8606.5	499	12	84
1773	G[81]	-8619.5	386	12	84
1774	G[79]	-8631.5	499	12	84
1775	G[77]	-8644.5	386	12	84
1776	G[75]	-8656.5	499	12	84
1777	G[73]	-8669.5	386	12	84
1778	G[71]	-8681.5	499	12	84
1779	G[69]	-8694.5	386	12	84
1780	G[67]	-8706.5	499	12	84
1781	G[65]	-8719.5	386	12	84
1782	G[63]	-8731.5	499	12	84
1783	G[61]	-8744.5	386	12	84
1784	G[59]	-8756.5	499	12	84
1785	G[57]	-8769.5	386	12	84
1786	G[55]	-8781.5	499	12	84
1787	G[53]	-8794.5	386	12	84
1788	G[51]	-8806.5	499	12	84
1789	G[49]	-8819.5	386	12	84
1790	G[47]	-8831.5	499	12	84
1791	G[45]	-8844.5	386	12	84
1792	G[43]	-8856.5	499	12	84
1793	G[41]	-8869.5	386	12	84
1794	G[39]	-8881.5	499	12	84
1795	G[37]	-8894.5	386	12	84
1796	G[35]	-8906.5	499	12	84
1797	G[33]	-8919.5	386	12	84
1798	G[31]	-8931.5	499	12	84
1799	G[29]	-8944.5	386	12	84
1800	G[27]	-8956.5	499	12	84

No.	Name	X-axis	Y-axis	W	H
1801	G[25]	-8969.5	386	12	84
1802	G[23]	-8981.5	499	12	84
1803	G[21]	-8994.5	386	12	84
1804	G[19]	-9006.5	499	12	84
1805	G[17]	-9019.5	386	12	84
1806	G[15]	-9031.5	499	12	84
1807	G[13]	-9044.5	386	12	84
1808	G[11]	-9056.5	499	12	84
1809	G[9]	-9069.5	386	12	84
1810	G[7]	-9081.5	499	12	84
1811	G[5]	-9094.5	386	12	84
1812	G[3]	-9106.5	499	12	84
1813	G[1]	-9119.5	386	12	84
1814	DUMMY[111]	-9131.5	499	12	84
1815	DUMMY[112]	-9144.5	386	12	84
1816	DUMMY[113]	-9156.5	499	12	84
1817	DUMMY[114]	-9169.5	386	12	84

13. REVISION HISTORY

Revision	Content	Page	Date
1.0.0	JD79665 datasheet 1st version	-	2023/08/25